HK32L08x/HK32L0Hx Datasheet

Version: 1.2

Release Date: 2023-01-31

Shenzhen Hangshun Chip Technology R&D Co., Ltd

http://www.hsxp-hk.com

Preface

Purpose

This document introduces the block diagram, memory mapping, peripheral interfaces, electrical characteristics, and pinouts of HK32L08x/HK32L0Hx Series SOC, to help users quickly understand its features and functions.

Audience

This document is intended for:

- Developer
- Tester

Release Notes

This document is corresponding to HK32L08x/HK32L0Hx Series SOC.

Revision History

Version	Date	Description
1.0	2022/11/07	Initial Release
1.1	2022/11/15	Update *Section 7.4 QFN32 and Section 7.5 QFN28.* Add the EXTI function in *Section 6.7 Pin function.*
1.2	2023/01/31	Update “6.7 pin definition” and the features of EEPROM.

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

Contents

1 Introduction 1
2 Overview 3
2.1 Features 3
2.2 Device Overview 6
3 Function Description 9
3.1 Block Diagram 9
3.2 Memory Mapping 10
3.3 Memory 10
3.3.1 Flash 10
3.3.2 SRAM 10
3.3.3 EEPROM 10
3.4 Power Supply Schemes 10
3.5 Power Monitor 11
3.6 Low-power Modes 11
3.7 Reset 12
3.7.1 System Reset 12
3.7.2 Power Reset 12
3.7.3 Backup Domain Reset 13
3.8 Clock and Clock Tree 13
3.9 SYSCFG 14
3.10 GPIO 14
3.11 DMA 14
3.12 Interrupt and Event 15
3.12.1 NVIC 15
3.12.2 EXTI 16
3.13 ADC 16
3.13.1 AWD Wake-up Function 17
3.13.2 Temperature Sensor 17
3.13.3 Internal Reference Voltage 17
3.14 DAC 17
3.15 Comparator 17

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

3.16 Operational Amplifier 17
3.17 EMACC 17
3.18 CLU 18
3.19 LCD 18
3.20 CRC Calculation Unit 18
3.21 DVSQ 18
3.22 Timer 19
3.22.1 Advanced Timer 19
3.22.2 General-purpose Timer 19
3.22.3 LPTIM 20
3.22.4 SysTick Timer 20
3.23 Independent Watchdog 20
3.24 Window Watchdog 20
3.25 RTC 21
3.26 ITRIM 21
3.27 USART/UART 21
3.28 LPUART 22
3.29 SPI/I2S 22
3.30 CAN 23
3.31 I2C Bus 23
3.32 USB 24
3.33 AWU Timer 24
3.34 Information Security 24
3.34.1 AES 24
3.34.2 TRNG 25
3.35 96-bit UID 25
3.36 Beeper 25
3.37 Debug Interface 25
4 Electrical characteristics 26
4.1 HK32L08x 26
4.1.1 Absolute maximum values 26
4.1.1.1 Voltage characteristics 26

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

4.1.1.2 Current characteristics 26
4.1.1.3 Thermal characteristics 26
4.1.2 Operation conditions 27
4.1.2.1 General operation conditions 27
4.1.2.2 PVD characteristics 27
4.1.2.3 BOR characteristics 27
4.1.2.4 POR/PDR characteristics 28
4.1.2.5 Embedded reference voltage 28
4.1.2.6 Operating current 28
4.1.2.7 High-speed external (HSE) RC oscillator 29
4.1.2.8 Low-speed external (LSE) RC oscillator 30
4.1.2.9 Middle-speed internal (MSI) RC oscillator 30
4.1.2.10 How-speed internal (HSI) RC oscillator 31
4.1.2.11 Low-speed internal (LSI) RC oscillator 31
4.1.2.12 PLL characteristics 31
4.1.2.13 EEPROM characteristics 32
4.1.2.14 Flash memory characteristics 32
4.1.2.15 I/O port input characteristics 32
4.1.2.16 I/O Output voltage characteristics 33
4.1.2.17 NRST reset pin characteristics 33
4.1.2.18 TIM characteristics 33
4.1.2.19 EMACC characteristics 33
4.1.2.20 ADC characteristics 34
4.1.2.21 DAC characteristics 36
4.1.2.22 Temperature sensor characteristics 37
4.1.2.23 Comparator characteristics 37
4.1.2.24 Operational amplifiers characteristics 37
4.1.2.25 LCD controller characteristics 38
4.2 HK32L0Hx 39
4.2.1 Absolute maximum values 39
4.2.1.1 Voltage characteristics 39
4.2.1.2 Current characteristics 39

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

4.2.1.3 Thermal characteristics 39
4.2.2 Operation conditions 39
4.2.2.1 General operation conditions 39
4.2.2.2 PVD characteristics 40
4.2.2.3 BOR characteristics 40
4.2.2.4 POR/PDR characteristics 40
4.2.2.5 Embedded reference voltage 41
4.2.2.6 Operating current 41
4.2.2.7 High-speed external (HSE) RC oscillator 41
4.2.2.8 Low-speed external (LSE) RC oscillator 42
4.2.2.9 Middle-speed internal (MSI) RC oscillator 43
4.2.2.10 How-speed internal (HSI) RC oscillator 43
4.2.2.11 Low-speed internal (LSI) RC oscillator 44
4.2.2.12 PLL characteristics 44
4.2.2.13 EEPROM characteristics 44
4.2.2.14 Flash memory characteristics 44
4.2.2.15 I/O port input characteristics 45
4.2.2.16 I/O Output voltage characteristics 45
4.2.2.17 NRST reset pin characteristics 46
4.2.2.18 TIM characteristics 46
4.2.2.19 EMACC characteristics 46
4.2.2.20 ADC characteristics 46
4.2.2.21 DAC characteristics 49
4.2.2.22 Temperature sensor characteristics 49
4.2.2.23 Comparator characteristics 49
4.2.2.24 Operational amplifiers characteristics 50
4.2.2.25 LCD controller characteristics 51
5 Typical circuitry 52
5.1 Power supply scheme 52
6 Pinouts and pin descriptions 53
6.1 LQFP64 53
6.2 LQFP48 54

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

6.3 LQFP32 55
6.4 QFN32 56
6.5 QFN28 56
6.6 TSSOP20 57
6.7 Pin definition 57
6.8 Alternate Function description 64
7 Package characteristics 67
7.1 LQFP64 67
7.2 LQFP48 68
7.3 LQFP32 69
7.4 QFN32 70
7.5 QFN28 71
7.6 TSSOP20 72
8 Ordering information 74
9 Glossary and Abbreviations 75
10 Legal and Contact Information 76

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

1 Introduction

This document is the datasheet for HK32L08x/HK32L0Hx series System-on-Chips (SOCs). HK32L08x/HK32L0Hx is a family of low-power microcontrollers (MCU) developed by Shenzhen Hangshun chip technology R&D Co., Ltd, including:

- HK32L08x subseries:
  - HK32L08xRBT6 (LQFP64 Package)
    - HK32L084RBT6
    - HK32L088RBT6 (with EEPROM)
  - HK32L08xCBT6 (LQFP48 Package)
    - HK32L084CBT6
    - HK32L088CBT6 (with EEPROM)
  - HK32L08xKBT6 (LQFP32 Package)
    - HK32L084KBT6
    - HK32L088KBT6 (with EEPROM)
  - HK32L08xKBU6 (QFN32 Package)
    - HK32L084KBU6
    - HK32L088KBU6 (with EEPROM)
  - HK32L08xGBU6 (QFN28 Package)
    - HK32L084GBU6
    - HK32L088GBU6 (with EEPROM)
  - HK32L08xFBP6 (TSSOP20 Package)
    - HK32L084FBP6
    - HK32L088FBP6 (with EEPROM)
- HK32L0Hx subseries:
  - HK32L0HxRBT6 (LQFP64 Package)
    - HK32L0H4RBT6
    - HK32L0H8RBT6 (with EEPROM)
  - HK32L0HxCBT6 (LQFP48 Package)
    - HK32L0H4CBT6
    - HK32L0H8CBT6 (with EEPROM)
  - HK32L0HxKBT6 (LQFP32 Package)
    - HK32L0H4KBT6
    - HK32L0H8KBT6 (with EEPROM)
  - HK32L0HxKBU6 (QFN32 Package)
    - HK32L0H4KBU6
    - HK32L0H8KBU6 (with EEPROM)
  - HK32L0HxGBU6 (QFN28 Package)
    - HK32L0H4GBU6
    - HK32L0H8GBU6 (with EEPROM)
  - HK32L0HxFBP6 (TSSOP20 Package)

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

- HK32L0H4FBP6
- HK32L0H8FBP6 (with EEPROM)

For details about these series MCUs, please refer to *HK32L08x/HK32L0Hx User manual.*

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

2 Overview

Based on ARM® Cortex®-M0 core, HK32L08x/HK32L0Hx embeds a 128-Kbyte Flash, a 20-Kbyte SRAM, and a 64Kbit EEPROM (optional), and operates up to 48MHz.

HK32L08x/HK32L0Hx supports the traditional Flash read/write protection, and Flash code encryption developed by Hangshun. Meanwhile, CRC, AES, and TRNG hardware computing units are provided to check data integrity, data encryption and decryption for different security applications.

HK32L08x/HK32L0Hx embeds multiple communication interfaces:

- A USB2.0 full-speed interface
- A CAN2.0A/2.0B interface
- 2 USARTs, 2 UARTs, and a LPUART
- 2 SPIs
- 2 I2Cs

HK32L08x/HK32L0Hx integrates a segment LCD driving circuit, to display low-power segment LCD.

HK32L08x/HK32L0Hx integrates a 16-bit advanced PWM timer (total of 4 PWM outputs, 3 of which can output complementary signals with dead time), five 16-bit general-purpose timers, a 32-bit general purpose timer, and three 16-bit low-power timers.

HK32L08x/HK32L0Hx integrates analog circuits: a 12-bit ADC (16 channels), a DAC (single channel), three analog operational amplifiers, two analog comparators, a power-on reset (POR)/power-down reset (PDR), a brown-out reset (BOR), a temperature sensor and an internal reference voltage (for internal ADC sampling).

HK32L08x/HK32L0Hx also integrates a hardware division square root unit (DVSQ) and a configurable logic unit (CLU), to enhance the capacity of software processing and fast response to external events.

Except for Power, Ground, and NRST pins, all the pins can be used as GPIOs, peripheral IOs, or external interrupt inputs. In application scenarios where the number of pins is limited, HK32L08x/HK32L0Hx provides as many pin functions as possible.

HK32L08x/HK32L0Hx supports multiple low-power consumption modes, which is fit for applications that have low-power requirements. The Device provides low-power Run mode, Sleep mode, Low-power Sleep mode, Stop mode and Standby mode.

Because of its various peripheral interfaces, HK32L08x/HK32L0Hx can be used in rich sets of applications. Examples of these applications include:

- Programmable controllers, printers, and scanners
- Motor drivers and speed control
- Low-power terminals with sensors for the Internet of Things
- UAV flight control, pylon control
- Toy products
- Household appliances
- Intelligent robots
- Smartwatches, sports bracelets

2.1 Features

- CPU core
  - ARM® Cortex®-M0 core

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

- Maximum frequency: 48MHz
- 24-bit SysTick timer
- Supports interrupt vector remapping (through configuring Flash registers)

- Operating voltage range
  - V_{DD}: 1.8 V to 4.2 V (HK32L08x)
  - V_{DD}: 2.7V to 5.5V (HK32L0Hx)
- Operating temperature range: -40°C to +85°C
- Typical operating current
  - Run mode: 3.2mA@8MHz@3.3V
  - Low Power Run mode: 8.8μA@32.768kHz@3.3V
  - Sleep mode: 201.4μA@32.768kHz@3.3V
  - Low Power Sleep mode: 5.0μA@32.768kHz@3.3V
  - Stop mode: 52.4μA @3.3V
  - Low-power Stop mode: 0.8μA @32.768kHz@3.3V
  - Standby mode: 0.2μA@3.3V
- Memory
  - 128 Kbytes Flash
    - Zero wait period to access Flash when CPU frequency is no more than 24MHz
    - Flash data security protection function (read or write protection can be set respectively)
    - Instructions and data stored in Flash encryption, to protect Flash content from physical attacks
  - 20 Kbytes SRAM
  - 64Kbit EEPROM (optional)
    - Cooperates with I2C2
- Clock
  - External high-speed clock (HSE): 4 - 24MHz
  - External low-speed clock (LSE): 32.768kHz
  - Internal high-speed clock (HSI): 8MHz (HSI)/16MHz (HSI16)/48MHz (HSI48)
  - Internal low-speed clock (LSI): 32.768kHz
  - PLL clock: 48 MHz (Max.)
  - External GPIO input clock: 48 MHz (Max.)
  - Middle-speed clock (MSI): 2.1MHz (default value, 5 configurable levels)
- Reset
  - External pin reset (NRST)
  - Window watchdog end of count reset (WWDG reset)
  - Independent watchdog end of count reset (IWDG reset)
  - Power reset (POR/PDR)
  - Software reset
  - Low-power management reset
  - Option byte loader reset
- Programmable voltage detector (PVD)
  - 8 configurable level detecting voltage thresholds

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

- Rising edge or falling edge detection
- GPIO
  - Up to 55 GPIOs
- Data communication interfaces
  - 2 x USARTs
    - RX and TX pins are swappable
    - Wake up the MCU from Stop mode when receiving any data frame
  - 2 x UARTs
  - 1 x LPUART
  - 2 x I2Cs
    - Communication speed: 1 Mbit/s, 400Kbit/s, or 100Kbit/s
    - Wake up the MCU from Stop mode when receiving any data
  - 2 x high-speed SPI/I2S (up to 18 Mbps)
  - 1 x 2.0A/2.0B CAN
  - 1 x USB2.0 full-speed device
- Timer
  - 1 x 16-bit advanced PWM timer (TIM1)
    - A total of 4 PWM outputs, 3 of which can output complementary signals with dead time
    - Supports break function
  - 6 x general-purpose timers
    - 1 x 32-bit general-purpose timer (TIM2)
    - 5 x 16-bit general-purpose timers (TIM3/TIM14/TIM15/TIM16/TIM17)
  - 3 x 16-bit low-power timers (LPTIM1/LPTIM2/LPTIM3)
    - Supports low-power Run mode, Sleep mode, low-power Sleep mode, and Stop mode
- DMA controller
  - 7 channels
  - Supports timer, SPI, I2C, USART, UART, LPUART, AES, ADC, and DAC
- Division and square root calculation
  - Supports 32-bit fixed point numbers division, the quotient and the remainder are available at the same time
  - Supports 32-bit fixed point numbers with high-precision square root
- 4 configurable logic units (CLU)
  - The pins of each CLU connect to the internal logic directly, to trigger on-chip sources
  - CLU supports combination logic function
- Electric motor accelerating unit (EMACC)
  - Supports Cordic operation for sine and cosine calculation
  - Supports Clarke, Park and anti-park operation
- Segment LCD controller
  - 4*32 or 8*28 pixels
  - Frame rate: 30-100Hz
  - LCD based on segments
- Real-time clock and calendar

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

- Programmable alarm
- Wake up the MCU periodically from Stop mode and Standby mode

- Data security
  - CRC parity hardware unit
  - Security encryption modules
    - AES
    - TRNG
- On-chip analog circuits
  - 1 x 12-bit SAR ADC (16 analog input channels)
    - Up to 1 MSPS (12-bit)
    - Supports differential input pairs
    - Auto continuous conversion, and scan conversion functions
  - Internal reference voltage
  - Temperature sensor
    - Output connects to the separate ADC input channel
  - 1 x 12-bit DAC (single channel)
  - 2 x voltage comparators
    - Each comparator can generate an interrupt signal, to wake up the MCU from the low-power mode.
    - Cooperates with DAC and timers to form periodical current controlling loop.
    - 2 comparators can work together with each other, and use as window comparators
  - 3 x operational amplifiers
- 96-bit UID
  - Used as a serial number and a security key
  - Activate security boot process
- CPU tracking and debugging
  - SWD debug interface
  - ARM® CoreSight™ debug component (ROM-Table, DWT, BPU)
  - Customized DBGMCU debug controller (low-power mode simulation controlling, the debug peripheral clock controlling, and debug and track interfaces allocating)
- Reliability
  - Passed HBM2500V/CDM1750V/LU350mA level tests.

2.2 Device Overview

Table 2-1 HK32L08x/HK32L0Hx features

Features	HK32L08xRBT6 HK32L0HxRBT6	HK32L08xCBT6 HK32L0HxCBT6	HK32L08xKBT6 HK32L0HxKBT6	HK32L08xKBU6 HK32L0HxKBU6	HK32L08xGBU6 HK32L0HxGBU6	HK32L08xFBP6 HK32L0HxFBP6
GPIO	55	39	26	26	24	16
Package	LQFP64	LQFP48	LQFP32	QFN32	QFN28	TSSOP20
Operating Voltage	HK32L08x: 1.8V-4.2V HK32L0Hx: 2.7V-5.5V					
Operating Temperature	-40°C - +85°C					

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

Features		HK32L08xRBT6 HK32L0HxRBT6	HK32L08xCBT6 HK32L0HxCBT6	HK32L08xKBT6 HK32L0HxKBT6	HK32L08xKBU6 HK32L0HxKBU6	HK32L08xGBU6 HK32L0HxGBU6	HK32L08xFBP6 HK32L0HxFBP6
Memory	Flash (Kbyte)	128					
	SRAM (Kbyte)	20					
	EEPROM (Kbit)	64 (Only HK32L088 and HK32L0H8 subseries provide)					
CPU	Core	Cortex®-M0					
	Frequency	48MHz					
DMA(number of channels)		1 (7 channels)					
DVSQ		1					
Clock	LSI	32.768kHz					
	HSI	8MHz/16MHz/48MHz					
	PLL	48MHz (Max.)					
	HSE	4-24MHz					
	LSE	32.768kHz					
Timer	Advanced Timer	1 (TIM1)					
	General-purpose Timer	1 x 32-bit timer: TIM2 5 x 16-bit timers TIM3/TIM14/TIM15/TIM16/TIM17					
	Low-power Timer	3 x 16-bit timers LPTIM1/LPTIM2/LPTIM3					
	System Tick	1					
	IWDG	1					
	WWDG	1					
Communication	USART	2					
	UART	2					
	LPUART	1	1	1	1	1	-
	I2C	2					
	SPI/I2S	2/2	2/2	1/1	1/1	1/1	1/1
	CAN	1					
	USB	1					
	Segment LCD	8com*28 segment/ 4com*32 segment	4 com*18 segment	-	-	-	-
CLU		4					
ITRIM		1					
ADC	ADC (Channels)	1 (16)	1 (10)	1 (10)	1 (10)	1 (10)	1 (9)

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

Features		HK32L08xRBT6 HK32L0HxRBT6	HK32L08xCBT6 HK32L0HxCBT6	HK32L08xKBT6 HK32L0HxKBT6	HK32L08xKBU6 HK32L0HxKBU6	HK32L08xGBU6 HK32L0HxGBU6	HK32L08xFBP6 HK32L0HxFBP6
	Internal reference voltage	1					
	ADC Sampling rate	1MSPS (12bit)					
	ADC Resolution	12-bit					
Temperature Sensor		1					
DAC (channels)		1 (1)					
Comparator		2					
Operational Amplifier		3					
EMACC		1					
PVD		1					
Beeper		1					
CRC		1					
96-bit UID		1					
AES		1					
TRNG		1					

Note: only HK32L088/HK32L0H8 subseries have 64Kbit EEPROM.

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

3 Function Description

3.1 Block Diagram

HK32L08x/HK32L0Hx integrates a 128 Kbytes Flash memory, to store procedure and data.

ARM® Cortex®-M0 is a 32-bit RISC processor, which provides a MCU platform with low-cost and low-power consumption features. It delivers outstanding computational performance and an advanced system response to interrupts. With its embedded ARM Cortex-M0 core, HK32L08x/HK32L0Hx family is compatible with ARM tools and software.

Take HK32L088RBT6 for example, the block diagram of HK32L08x/HK32L0Hx shows as follows:

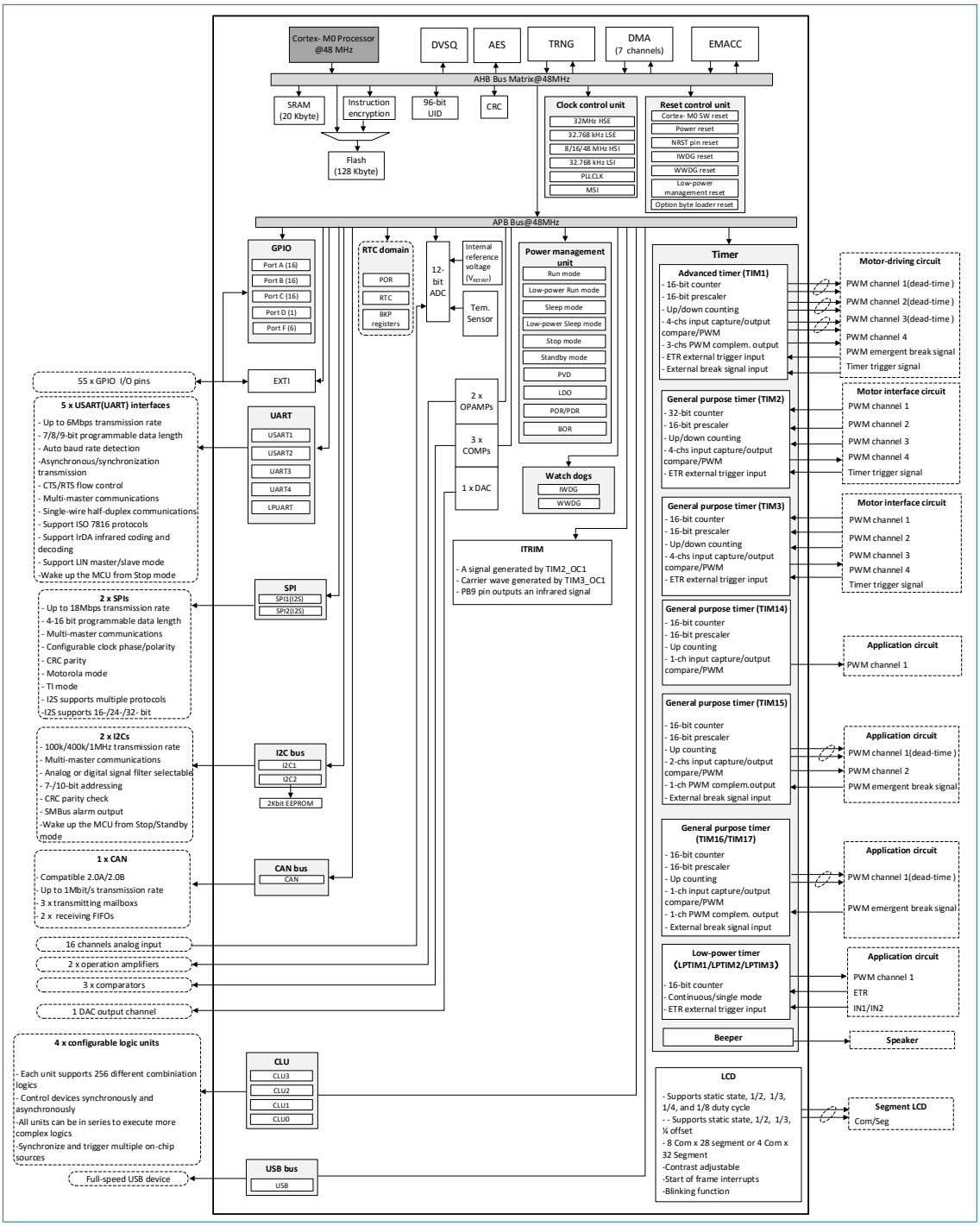


Figure 3-1 HK32L088RBT6 block diagram

3.2 Memory Mapping

Take HK32L088RBT6 for example, memory mapping of HK32L08x/HK32L0Hx shows as follows:

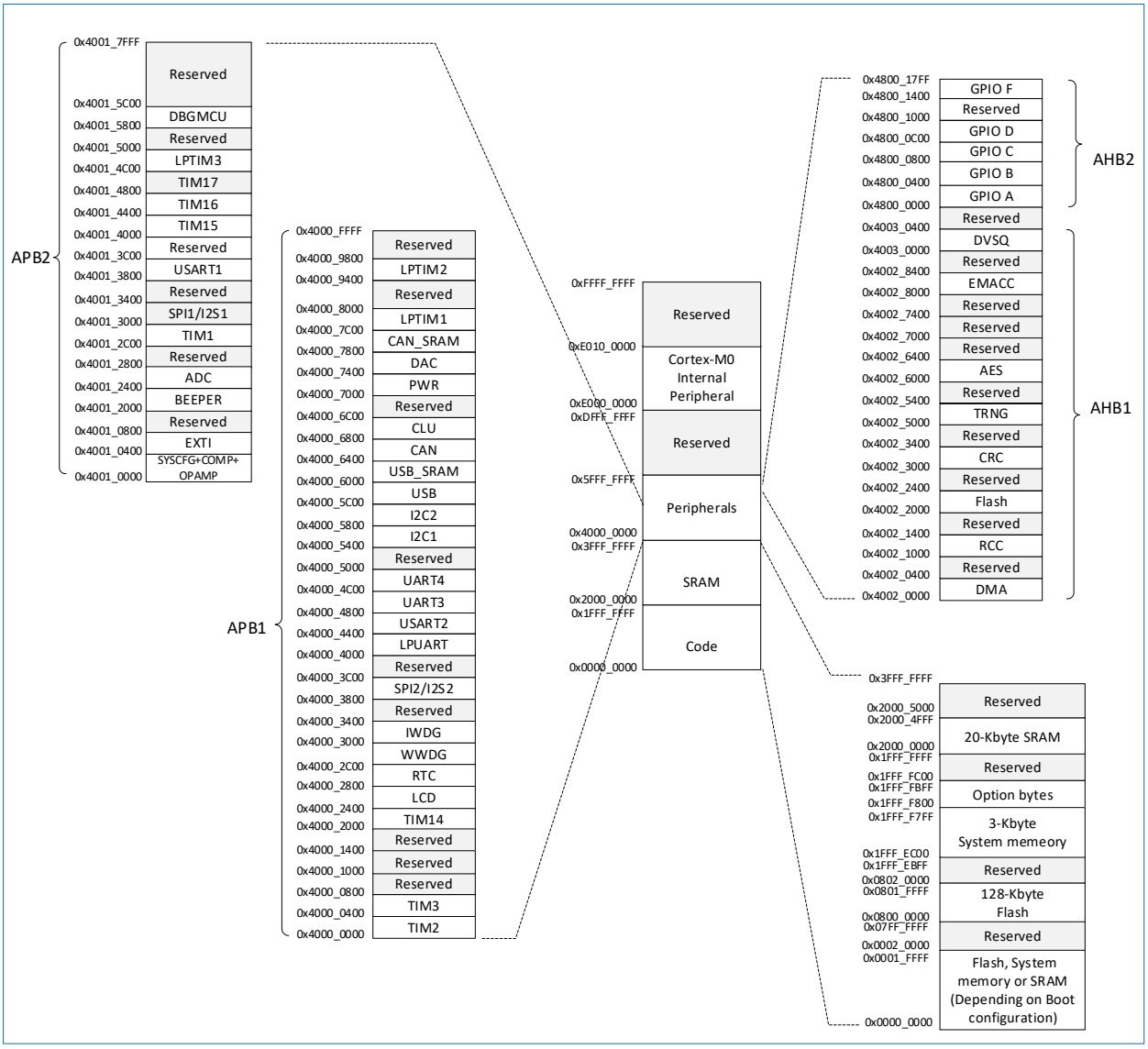


Figure 3-2 Memory mapping

3.3 Memory

3.3.1 Flash

HK32L08x/HK32L0Hx integrates a 128Kbyte Flash for storing procedure and data, which supports interrupt vector table remapping by configuring Flash registers.

3.3.2 SRAM

HK32L08x/HK32L0Hx integrates a 20-Kbyte SRAM, and supports read/write access in word, half-word and byte. CPU can access SRAM fast with zero wait period to meet the requirements of most applications.

3.3.3 EEPROM

HK32L088 and HK32L0H8 subseries integrate a 64Kbit EEPROM, which must cooperate with I2C2.

3.4 Power Supply Schemes

- HK32L08x

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

- V_{DD}=1.8-4.2V: external single power supply (without V_{BAT}) for digital circuits, I/Os, and the internal regulator. When powering on, V_{DD} should more than 1.9V. After powered on, that V_{DD} drops down to 1.8V is permitted.
- V_{SSA},V_{DDA}=1.8-4.2V: external analog power supply for ADC, DAC, RC oscillator, etc. V_{SSA} and V_{DDA} must be connected to V_{DD} and V_{SS} respectively。

- HK32L0Hx
  - V_{DD}=2.7V-5.5V: external single power supply (without V_{BAT}) for digital circuits, I/Os, and the internal regulator.
  - V_{SSA},V_{DDA}=2.7V-5.5V: external analog power supply for ADC, DAC, RC oscillator, etc. V_{SSA} and V_{DDA} must be connected to V_{DD} and V_{SS} respectively。

3.5 Power Monitor

Device integrates a POR (Power-on reset)/PDR (Power-down reset)/BOR (Brown-out reset) circuitry. POR/PDR and BOR act as a double protection function, to assure the system working when power supply is over 1.8V/2.7V (depending on MCU models). When V_{DD} is below the threshold of POR/PDR or that of BOR, device is reset., without the need for an external reset circuitry.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. The V_{PVD} threshold is programmable via software. When V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold, an interrupt can be generated. The interrupt routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.6 Low-power Modes

HK32L08x/HK32L0Hx supports several low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources.

- Low-power run mode

In Low-power run mode, clock frequency (LSE or LSI) is below 131kHz. Meanwhile, the LDO switches to the low-power mode.

- Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- Low power Sleep mode

In Low-power Sleep mode, only the CPU is stopped, the voltage regulator runs in the low-power mode (the clock frequency is lower), only some peripherals work and the MCU can be woken up from this mode when an interrupt or an event arrives.

- Stop mode

Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. In Stop mode, all internal clocks, PLL, HSI, and HSE oscillators are disabled. MCU can be woken up from Stop mode by any EXTI line. The EXTI line source can be any one of external I/O pins, the PVD output, the RTC alarm or the USB wakeup signal.

- Standby mode

Standby mode achieves the lowest power consumption. CPU and the main digital logics are off, only the power management circuit is on. PLL, HSI, HSE, MSI, LSI oscillators are off. After entering Standby mode, the content of SRAM and registers disappeared, but the content of backup registers is retained, and standby circuitry is still working.

The conditions of exiting from Standby mode include: an external reset signal on NRST pin, IWDG reset, a rising edge on WKUP pin or RTC timer counting to end.

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

3.7 Reset

HK32L08x/HK32L0Hx supports System reset and Power reset.

3.7.1 System Reset

Except for the reset flag bits in the RCC_CSR register and registers in the backup domains, the system reset signal resets all the registers.

Users can identify reset sources by checking the reset flag bits in the RCC_CSR register.

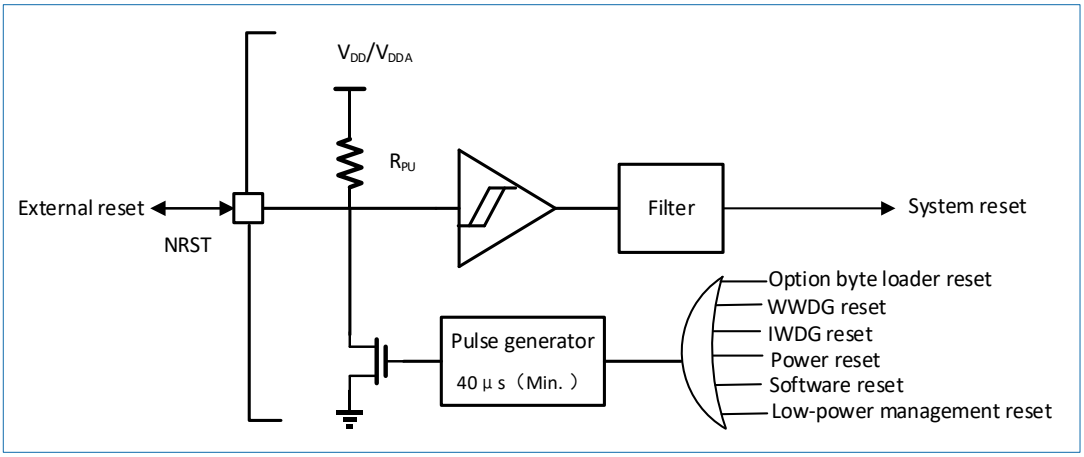


Figure 3-3 Reset

When any of the following events occurs, a system reset signal is generated:

- Low level on NRST pin (External Reset)
- Option byte loader reset
- Window watchdog counting terminates (WWDG Reset)
- Independent watchdog counting terminates (IWDG Reset)
- Software reset (SW Reset): by setting SYSRESETREQ bit to ‘1’ or Cortex-M0 interrupt to perform Software reset.
- Low-power management reset

Reset source signals effect on NRST pin at last, and keep it low level during reset. Reset entry vector is fixed at address 0x0000 0004. An internal reset signal outputs on NRST pin. A Pulse generator ensures that each reset source produces at least 40 us pulse latency. When NRST pin is pulled down and a reset pulse is generated for an external reset.

3.7.2 Power Reset

When the following event occurs, Power reset signal is generated:

- POR/PDR
- BOR
- Return from Standby mode

HK32L08x/HK32L0Hx embeds a POR/PDR circuitry. The circuitry always operates to ensure the system runs well when the power supply is over 1.8V/2.7V. When V_{DD} is less than the POR/PDR threshold, MCU resets and no external reset circuitry is required.

HK32L08x/HK32L0Hx embeds a BOR circuitry. BOR is turned off by default, power supply is monitored by POR/PDR. Users can enable the BOR function by configurating the option bytes.

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

3.7.3 Backup Domain Reset

The backup domain has two special resets, which effect on the backup domain.

The backup domain resets by any one of the following events:

- Software reset, triggered by the BDRST bit of the RCC_BDCR register in the backup domain.
- V_{DD} is powered on again after V_{DD} is powered down.

3.8 Clock and Clock Tree

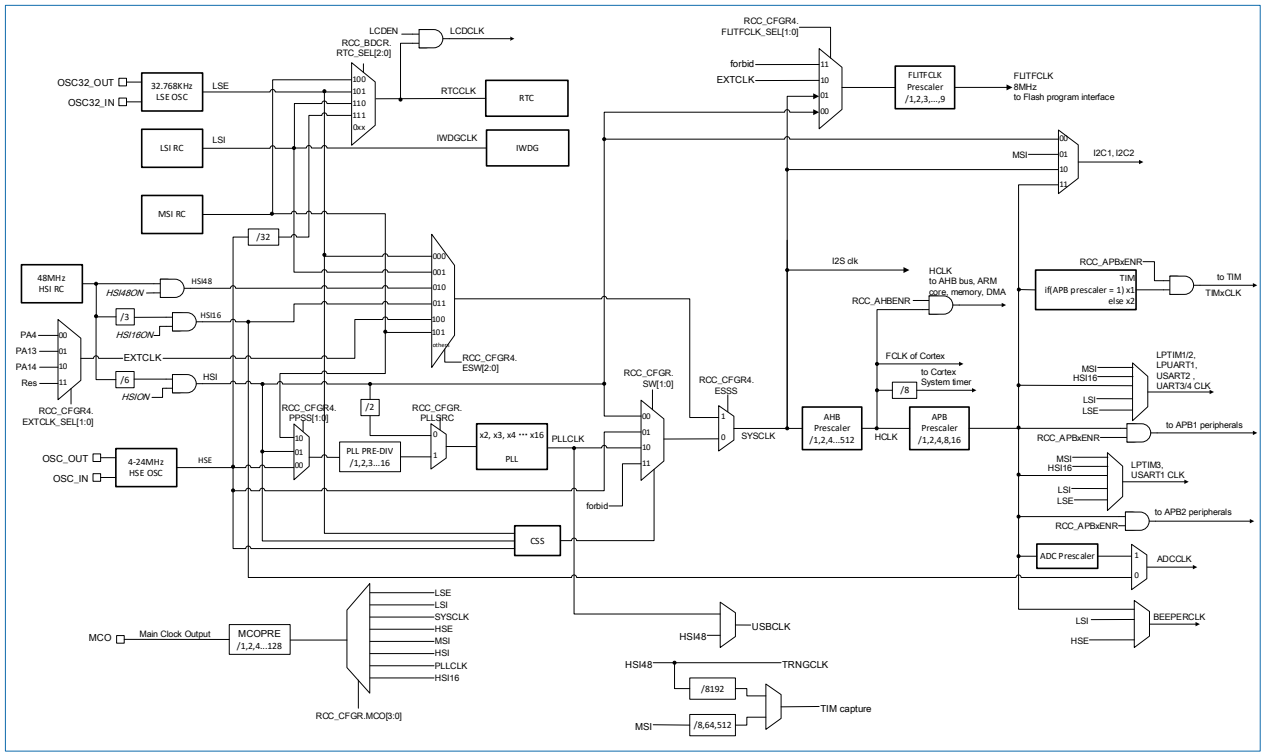


Figure 3-4 Clock tree

As shown in the figure above, HSI and HSI16 is clocked from the 48 MHz internal oscillator. Thus, when using HSI or HSI16 clock, the other one can not be turned off to reduce power consumption. HSI or HSE can act as the input of the PLL prescaler. By using HSI and PLL together, more system clock frequencies can be offered.

HK32L08x/HK32L0Hx selects a system clock as the CPU clock when it starts. When it resets, 8MHz HSI RC is selected as the system clock by default.

HK32L08x/HK32L0Hx can select one of the multiple clock sources as the system clock:

- High-speed external clock (HSE): 4-24MHz
- Low-speed external clock (LSE): 32.768kHz
- High-speed internal clock: 8MHz (HSI)/16MHz (HSI16)/48MHz (HSI48)
- Low-speed internal clock (LSI): 32.768kHz
- PLL clock: 25-48MHz
- External GPIO input clock: 48MHz (Max.)
- MSI clock: 2.1MHz (default value, 5 programmable levels)

The MSI clock is a low-cost and low-power clock source, which can be used as a wakeup clock in the low-power mode.

Clock frequencies of AHB bus and APB domain can be set by several prescalers. The max clock frequency of AHB bus and APB domain is 48MHz.

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

Clock security system can monitor the faults of HSE and LSE, and can switch the clock source when detecting the faults.

3.9 SYSCFG

Device has a set of the SYSCFG registers. System configuration registers are used for:

- Enable/disable I2C1 fast mode plus mode on some I/Os.
- Swapping the remapping functions of Some GPIOs
- Remapping some DMA trigger sources to other DMA channels
- Remapping the memory located at the beginning of the code area
- Managing the external interrupt line connection to the GPIOs
- Managing robustness feature
- Decoupling LCD power cable
- Managing the temperature sensor and the internal reference voltage

3.10 GPIO

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate functional. Most of GPIO pins are shared with digital or analog alternate functional. All GPIOs are high current capable. The alternate function of I/Os can be locked in order to avoid spurious writing to the I/O registers.

VDDIO2 supplies power for USB and some GPIOs.

Figure 3-5 VDDIO2 power domain

Package		VDDIO2 power domain											
		PA8	PA9	PA10	PA11	PA12	PA13	PA14	PA15	PC10	PC11	PC12	PF6
LQFP64		●	●	●	●	●	●	●	●	●	●	●	●
LQFP48		●	●	●	●	●	●	●	●	-	-	-	●
LQFP32	When LCD function is unavailable	●	●	●	●	●	●	●	●	-	-	-	-
	When PA8 function is unavailable	-	●	●	●	●	●	●	●	-	-	-	-
QFN28		-	●	●	-	-	●	●	●	-	-	-	-

- “●” in above table represents supporting.

3.11 DMA

The flexible general-purpose DMA manage the transfers from memories to memories, peripherals to memories, and memories to peripherals. Data is transferred from the source address to the destination address, without any CPU action. This keeps CPU resources free for other operations.

- Memories to memories accesses
- Peripherals to memories, and memories to peripherals accesses
- Up to 7 channels
- Each channel connects to dedicated hardware and can be triggered by this hardware or software.
- Supports circular buffer management.
- Supports DMA requests from ADC, SPI1/2, USART1/2, LPUART1, I2C1/2, TIM1/2/3/16/17, AES, DAC, and

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

UART3/4.

3.12 Interrupt and Event

3.12.1 NVIC

HK32L08x/HK32L0Hx embeds a nested vectored interrupt controller to handle 32 maskable interrupt channels (not including 16 Cortex®-M0 interrupt lines) and 4 interrupt priority levels flexibly with the low interrupt latency.

- Closely coupled NVIC gives low latency interrupt processing.
- Interrupt entry vector address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Supports for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

Table 3-1 NVIC

Position	Priority		Name	Description	Address
-	-	-	-	Reserved	0x0000 0000
-	-3	Fixed	Reset	Reset	0x0000 0004
-	-2	Fixed	NMI	Non-maskable interrupt The RCC Clock Security System (CSS) is linked to the NMI vector.	0x0000 0008
-	-1	Fixed	HardFault	All class of fault	0x0000 000C
-	3	Settable	SVCall	System service call via SWI instruction	0x0000 002C
-	5	Settable	PendSV	Pendable request for system service	0x0000 0038
-	6	Settable	SysTick	System tick timer	0x0000 003C
0	7	Settable	WWDG	Window Watchdog interrupt	0x0000 0040
1	8	Settable	PVD	PVD interrupt (Combined with EXTI line 16)	0x0000 0044
2	9	Settable	RTC	RTC global interrupt (RTC alarm combined with EXTI line 17, RTC tamper, timestamp and CSS_LSE combined with EXTI line 19, RTC wakeup interrupt combined with EXTI line 20)	0x0000 0048
3	10	Settable	FLASH	Flash global interrupt	0x0000 004C
4	11	Settable	RCC	RCC global interrupt	0x0000 0050
5	12	Settable	EXTI0_1	EXTI Line[1:0] interrupt	0x0000 0054
6	13	Settable	EXTI2_3	EXTI Line[3:2] interrupt	0x0000 0058
7	14	Settable	EXTI4_15	EXTI Line[15:4] interrupt	0x0000 005C
8	15	Settable	LPUART	LPUART interrupt, combined with EXTI line 28	0x0000 0060
9	16	Settable	DMA_CH1	DMA Channel 1 global interrupt	0x0000 0064
10	17	Settable	DMA_CH2_3	DMA Channel 2 and 3 interrupt	0x0000 0068
11	18	Settable	DMA_CH4_7	DMA Channel 4/5/6/7 interrupt	0x0000 006C
12	19	Settable	ADC_COMP1_2	ADC and Comparator1/2 interrupt, ADC interrupt is combined with EXTI line 30, and comparator 1/2 is combined with EXTI line 21/22 respectively.	0x0000 0070
13	20	Settable	TIM1	TIM1 global interrupt	0x0000 0074
14	21	Settable	UART3_4	UART3/4 global interrupt	0x0000 0078

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

Position	Priority		Name	Description	Address
15	22	Settable	TIM2	TIM2 global interrupt	0x0000 007C
16	23	Settable	TIM3	TIM3 global interrupt	0x0000 0080
17	24	Settable	DAC	DAC interrupt	0x0000 0084
18	25	Settable	LPTIM1_3	LPTIM1/2/3 global interrupt, LPTIM1 combined with EXTI line 29, LPTIM2 combined with EXTI line 27, LPTIM3 combined with EXTI line 30	0x0000 0088
19	26	Settable	TIM14	TIM14 global interrupt	0x0000 008C
20	27	Settable	TIM15	TIM15 global interrupt	0x0000 0090
21	28	Settable	TIM16	TIM16 global interrupt	0x0000 0094
22	29	Settable	TIM17	TIM17 global interrupt	0x0000 0098
23	30	Settable	I2C1	I2C1 global interrupt, combined with EXTI line 23	0x0000 009C
24	31	Settable	I2C2	I2C2 global interrupt, combined with EXTI line 24	0x0000 00A0
25	32	Settable	SPI1	SPI1 global interrupt	0x0000 00A4
26	33	Settable	SPI2	SPI2 global interrupt	0x0000 00A8
27	34	Settable	USART1	USART1 global interrupt, combined with EXTI line 25	0x0000 00AC
28	35	Settable	USART2	USART2 global interrupt, combined with EXTI line 26	0x0000 00B0
29	36	Settable	AES_TRNG_EMACC	AES/TRNG/EMACC global interrupt	0x0000 00B4
30	37	Settable	LCD_CAN	LCD and CAN global interrupt	0x0000 00B8
31	38	Settable	USB_DVSQ	USB, DVSQ global interrupt, and USB wakeup interrupt, combined with EXTI line 18	0x0000 00BC

3.12.2 EXTI

External interrupt/event controller (EXTI) manages internal and external asynchronous interrupts and events, including outputting an event request to CPU, an interrupt request to the interrupt controller, and a wakeup request to the power management unit.

Depending on whether the interrupt/event trigger edge is configurable, EXTI can be divided into two types: the configurable trigger edge EXTI or the fixed trigger edge EXTI. The fixed EXTI is triggered on a rising edge, only works in Stop mode, to wake up the core form Stop mode.

- Supports up to 32 event/interrupt requests
  - 22 configurable EXTI lines
    - A programmable trigger edge on rising or falling edge
    - Dedicated interrupt state flag
    - Interrupts or events can be triggered by software
  - 10 fixed EXTI lines
- Each interrupt/event line can be triggered and masked respectively.
- The EXTI can detect an external line with a pulse width shorter than the internal clock period.

3.13 ADC

Device integrates a 12-bit analog/digital converter with 16 external and 4 internal channels, which can be extended to 16 bits by oversampling. The A/D conversion of the channels can be performed in single, continuous, scan or discontinuous mode. ADC is low-power consumption in all clock frequencies adopted.

- ADC clock can be independently from the CPU clock. Even when the CPU runs in low speed, ADC sampling rate can up to 1MSPS.
- Automatically powered off except during the active conversion phase.

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

- ADC can work normally when the power supply voltage drops to the lowest MCU voltage permitted.
- Supports DMA
- Supports the wakeup function of analog watchdog in Stop mode.
- The events generated by TIM1, TIM2, or TIM3 connect to the ADC and trigger it, which make applications synchronize analog-digital conversion and the clock.
- Supports the differential input mode, the oven channel and the odd channel adjacent make up to a differential channel, such as AIN8 and AIN9.

3.13.1 AWD Wake-up Function

In Stop mode, system times by the beeper and sends a signal to ADC; ADC samples the signal to wake up the ADC clock. The ADC clock gets ready to trigger the ADC conversions and generates an AWD event according to ADC conversion results. An AWD event is sent to an EXTI line to wake up the system.

3.13.2 Temperature Sensor

The temperature sensor is used to detect the temperature around the device.

3.13.3 Internal Reference Voltage

The internal reference voltage (V_{REFINT}) provides a stable (bandgap) voltage output for ADC.

3.14 DAC

Device integrates a 12-bit, voltage output digital-to-analog converter with a buffer. DAC features:

- A data storage register
- Left or right data alignment in 12-bit mode
- Noise-wave generation
- Triangular-wave generation
- DMA capability for each channel
- External triggers for conversion

3.15 Comparator

Device embeds two ultra-low-power consumption comparators (COMP1 and COMP2). Each of them can be used as an independent device (with I/Os), or used with timers.

- Wake up the system from the low-power mode when triggered by an analog signal.
- Analog signal conditioning
- Combined with DAC and the PWM outputs of timers to form a cycle-by-cycle current control loop.

3.16 Operational Amplifier

Operational amplifiers (OPAMP) can be configured flexibly. The three internal operational amplifiers can be configured as a follower or as an amplifier with inverting or non-inverting gain, or can be used in parallel with the external resistors.

3.17 EMACC

Electric motor acceleration unit (EMACC) is used for brushless DC motors controlled by field oriented control (FOC) algorithm. EMACC can accelerate arithmetical operations of motor driving, its operating speed is faster than pure software. EMACC reduces CPU utilization and supports the faster motor speed.

Device has the hardware units corresponding to the calculations that occupy a lot of the CPU resource in FOC algorithms, such as Cordic, Clarke, Park, anti-Park, and PID. EMACC can reduce the FOC calculation time.

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

3.18 CLU

Device integrates a configurable logic module. It features:

- Four configurable logic units (CLUs), with direct-pin and internal logic connections.
- Each unit supports lots of combinatorial logic functions (AND, OR, XOR, multiplexing etc.), and contains a clocked flip-flop for synchronous operations.
- Supports synchronous and asynchronous operations.
- CLUs may be cascaded together to perform more complicated logic functions.
- Can operate in conjunction with serial peripherals such as UART and SPI or timing peripherals such as timers.
- Can be used to synchronize and trigger multiple on-chip resources (ADC, DAC, timers, etc.).
- Asynchronous output may be used to wake from low-power states.

3.19 LCD

Device embeds a digital controller/driver for liquid crystal display (LCD) with up to 4*32 or 8*28 pixels. LCD features:

- A step-up converter is embedded to generate the voltage for LCD. V_{LCD} supplies power , when the converter is disabled.
- Supports static, 1/2, 1/3, 1/4 and 1/8 duty.
- Supports static, 1/2, 1/3, and 1/4 bias.
- Blink capability: up to 1, 2, 3, 4, 8 or all pixels which can be programmed to blink at a configurable frequency.
- Double buffered memory allows data in LCD_RAM registers to be updated at any time.
- The LCD controller can be displayed in low-power mode.
- Supports V_{LCD} decoupling function.
- Highly flexible frame rate control.
- The contrast can be adjusted.
- The software can adjust V_{LCD} between V_{LCDmin} and V_{LCDmax}.
- Start of frame interrupt.

3.20 CRC Calculation Unit

CRC is used to verify data transmission or storage integrity. HK32L08x/HK32L0Hx integrates a CRC calculation unit to reduce user applications processing burden and to provide the ability to accelerate processing.

CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.21 DVSQ

Division and square root calculation (DVSQ) unit features:

- Supports 32-bit signed/unsigned number division and 32-bit unsigned number square root operations.
  - DVSQ unit supports only one type calculation each time, either division or square root.
  - Once a 32-bit signed/unsigned integer division operation completes, its quotient and the remainder are obtained simultaneously and updated in the corresponding register.
  - Division operations support MOD operating.
- Unsigned number square root operations can be set by software to operate with high precision.

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

- Pipeline design: 2-bit calculation is completed in every clock period.
- Calculation time depends on data in the operation.
- Supports dividing by zero interrupts and overflow interrupts

3.22 Timer

HK32L08x/HK32L0Hx has an advanced timer, six general-purpose timers and three low-power timers.

Table 3-2 Timer features

Timer type	Timer	Counter resolution	Counting type	Perscaler factor	DMA request generation	Break input	Capture/ Compare channel	Compensation output
Advanced timer	TIM1	16-bit	Up, down up/down	1-65536	Yes	Yes	4	3
General-purpose timer	TIM2	32-bit	Up, down up/down	1-65536	Yes	-	4	-
	TIM3	16-bit	Up, down up/down	1-65536	Yes	-	4	-
	TIM14	16-bit	Up	1-65536	-	-	1	-
	TIM15	16-bit	Up	1-65536	-	Yes	2	1
	TIM16	16-bit	Up	1-65536	Yes	Yes	1	1
	TIM17	16-bit	Up	1-65536	Yes	Yes	1	1
Low-power timer	LPTIM1	16-bit	Up	1/2/4.../ 128	-	-	1	-
	LPTIM2	16-bit	Up	1/2/4.../ 128	-	-	1	-
	LPTIM3	16-bit	Up	1/2/4.../ 128	-	-	1	-

3.22.1 Advanced Timer

HK32L08x/HK32L0Hx integrates an advanced timer (TIM1). TIM1 supports DMA.

The advanced timer can be seen as a three-phase PWM with 6 channels, and used as a complete general-purpose timer. The 4 independent channels can used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output
- Complementary PWM outputs with programmable inserted dead-times

If configured as a standard 16-bit timer, TIM1 has the same functions as the general-purpose timer. If configured as a 16-bit PWM generator, it has full modulation capability (0-100%). Because most of its internal structure is the same as that of a general-purpose timer. The advanced timer can work together with general-purpose timers via Timer Link feature for synchronization or event chaining. In debug mode, the counter can be frozen.

3.22.2 General-purpose Timer

HK32L08x/HK32L0Hx integrates six general-purpose timers.

- TIM2 and TIM3

TIM2 is based on a 32-bit auto-reload up/down counter and a 16-bit prescaler. TIM3 is based on a 16-bit auto-

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

reload up/down counter and a 16-bit prescaler. TIM2 and TIM3 have 4 independent channels respectively. Each channel is used for input capture/output compare, PWM or one-pulse mode output.

TIM2 and TIM3 can cooperate with advanced timers through Timer Linking feature for synchronization and event chaining. TIM2 and TIM3 can generate independent DMA requests. TIM2 and TIM3 are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors. In debug mode, their counters can be frozen.

- TIM14 and TIM15

TIM14 and TIM15 are based on a 16-bit auto-reload up counter and a 16-bit prescaler. TIM14 features one channel for input capture/output compare, PWM or one-pulse mode output. TIM15 features two channels, and one channel with complementary outputs. In debug mode, the counters can be frozen. TIM14 and TIM15 can't generate independent DMA requests.

- TIM16 and TIM17

TIM16 and TIM17 are based on a 16-bit auto-reload up counter and a 16-bit prescaler. TIM16 and TIM17 features one channel each for input capture/output compare, PWM or one-pulse mode output. TIM16 and TIM17 have complementary outputs, dead-time and independent DMA requests generation. In debug mode, their counters can be frozen.

3.22.3 LPTIM

HK32L08x/HK32L0Hx integrates three low-power timers (LPTIM1/LPTIM2/LPTIM3).

LPTIM can operate in Sleep mode and Stop mode. Without the internal clocks, LPTIM can provide the pulse counting function. LPTIM wakes up the MCU from low-power mode.

LPTIM provides more flexible clock scheme (LSE/LSI/HSI16/APB/MSI clock), to reduce power consumption.

Each LPTIM embeds a 16-bit auto-reload up counter and a 16-bit prescaler. Each LPTIM has one channel for input capture/output compare.

3.22.4 SysTick Timer

SysTick timer is dedicated to the operation system as a standard down counter. It features:

- 24-bit down counter
- Auto-reload capability
- Generate a maskable interrupt when the counter reaches 0.
- Programmable clock source

3.23 Independent Watchdog

Independent watchdog (IWDG) is clocked from an internal independent RC oscillator (LSI). The IWDG is based on a 12-bit down counter and an 8-bit prescaler. Because it is independently from the main clock, IWDG can operate in Stop mode and Standby mode. It can be used as a watchdog to reset the system when a problem occurs or as a free running timer for application timeout management. IWDG can be configured to a software or hardware watchdog through configuring option bytes. In debug mode, the counter can be frozen.

By configuring the IWDG_WINR register, IWDG can operate in the window mode.

3.24 Window Watchdog

Window watchdog (WWDG) is based on a 7-bit down counter. The counter can be set to the free running mode or used as a watchdog to reset the system when a problem occurs. It is clocked from the main clock and has an early warning interrupt capability. In debug mode, the counter can be frozen.

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

3.25 RTC

Real-time clock (RTC) contains an independent BCD timer/counter. Its features as below:

- Calendar with sub-seconds, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms with wakeup from Stop and Standby mode capability.
- Resolution is programmable and a periodic wakeup interrupt can be generated.
- On-the-fly correction from 1 to 32767 RTC clock pulses. It can synchronize the RTC with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 1 ppm resolution, to compensate the quartz crystal deviation.
- Two anti-tamper detection pins with programmable filter. When a tamper event is detected, the MCU can be woken up from Stop/Standby mode.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop/Standby mode on timestamp event detection.
- Timestamp function for event saving
- Tamper events with the configurable filter and internal pull-up.
- Maskable interrupts/events:
  - Alarm A
  - Alarm B
  - Wakeup interrupt
  - Timestamp
  - Tamper detection
- The RTC clock source
  - 32.768 kHz LSE
  - MSI
  - 32.768 kHz LSI
  - HSE/32

3.26 ITRIM

Device integrates an ITRIM. ITRIM should cooperate with infrared LED to realize remote control. To generate infrared remote control signals, enable the IRTIM interface (PB9 pin) and configure the channel 1 of TIM2 (TIM2_OC1) and the channel 1 of TIM3 (TIM3_OC1).

Configuring the timer to the input capture mode is easy to realize the infrared receiver function.

3.27 USART/UART

HK32L08x/HK32L0Hx embeds 4 universal synchronous/asynchronous receiver transmitters (USART1/USART2/UART3/UART4). The interfaces are able to communicate at speed of up to 6 Mbit/s.

The USARTs support CTS, RTS, RS485DE, multi-processor communications, master synchronous communications and single-wire half-duplex communications.

The USART interfaces provide Smart Card mode (ISO 7816 compliant), IrDA SIR ENDEC, and have LIN Master/Slave capability and automatic Baud rate detection.

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

The USART interfaces can use a clock domain independent from CPU clock to wake up the MCU in Stop mode.

Table 3-3 USART/UART features

USART features	USART1/USART2	UART3/UART4
Data word length	7-/8-/9-bit	7-/8-/9-bit
DMA	Yes	Yes
Multi-processor communication	Yes	Yes
Synchronous mode	Yes	No
Single-wire half-duplex communication	Yes	Yes
Dual clock domain and wake up from Stop mode	Yes	No
Auto-baudrate detection	Yes	No
Modbus communication	Yes	No
RS232 hardware flow control	Yes	Yes
RS485 driver enable	Yes	Yes
IrDA SIR ENDEC	Yes	No
LIN mode	Yes	No
Smart Card mode	Yes	No

3.28 LPUART

HK32L08x/HK32L0Hx embeds a low-power universal asynchronous receiver transmitter (LPUART). It communicates at speed of up to 10 Mbit/s.

The LPUART supports asynchronous serial communications, single-wire half-duplex communications, and modem operations (CTS and RTS). It also supports multiprocessor communication.

The LPUART clock domain is independent from the CPU clock. The system can be waked up from Stop mode. The wakeup events include:

- Detecting a start bit
- Receiving a data frame interrupt
- Receiving a specific programming data frame

The LPUART communicates up to 9600 baud when using LSE clock. In Stop mode, LPUART can operate in low-power state to wait for receiving the incoming frames.

The LPUART supports DMA.

3.29 SPI/I2S

HK32L08x/HK32L0Hx has two SPI interfaces, up to 18 Mbit/s communication speed and supports Master/Slave mode, full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies. Each frame can be configured to 4 bits or 16 bits. SPI supports CRC, TI mode and so on.

Table 3-4 SPI1/SPI2 features

SPI features	SPI1/SPI2
Hardware CRC calculation	Yes
RX/TX FIFO	Yes
NSS pulse mode	Yes
I2S mode	Yes
TI mode	Yes

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

SPI features	SPI1/SPI2
DMA	Yes

The standard I2S interface (multiplexed with SPI) supports 4 different audio standards and master/slave half-duplex communication mode. The I2S interface can be configured to 16/24/32 bits transmission and operates with 16/32 bits resolution. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When operating in master mode, the I2S interface can output the master clock to external DAC/CODEC at 256 times the sampling frequency.

Table 3-5 I2S features

I2S features	I2S1/I2S2
Half dual-duplex mode	Yes
Master/slave mode	Yes
8-bit programmable linear prescaler	Yes
Programmable data format	Yes
Programmable clock polarity	Yes
I2S protocols	Yes
DMA	Yes
Drive an external audio component	Yes

3.30 CAN

The CAN interface is compliant with Specification 2.0A and 2.0B (active). Its bit speed rate is up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has 3 transmit mailboxes and 2 receive FIFOs with 3 stages 14 scalable filter banks.

3.31 I2C Bus

The I2C bus interfaces can work as a master or as a slave and supports standard (100kbit/s), fast mode (400kbit/s) and fast mode plus (up to 1Mbit/s).

The I2C interfaces support SMBus V2.0/PMBus 1.1, including the address resolution protocol (ARP) capability, host notification protocols, packet error checking (PEC) generation/verification, timeout verification, and ALERT protocol management.

The I2C has a clock which is independent from the CPU clock domain, thus the I2C is able to wake up MCU from Stop mode when the addresses match.

When I2C2 operates in master mode, you can configure registers to access external slave devices or EEPROM.

Note: Only HK32L088 and HK32L0H8 subseries provide EEPROM.

Table 3-6 I2C features

I2C features	I2C1/I2C2
Master/Slave mode	Yes
Multi-master mode	Yes
Standard/Fast/Fast plus mode	Yes
7-bit/10-bit addressing	Yes
Broadcast call	Yes
Event management	Yes
Clock stretching	Yes

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

I2C features	I2C1/I2C2
Software reset	Yes
DMA	Yes
Digital and analog filter	Yes
SMBUS2.0	Yes
PMBUS1.1	Yes
Independent clock	Yes
Wake up from Stop mode	Yes

3.32 USB

Device embeds a USB device peripheral compatible with USB full-speed. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock for USB is generated by the internal main PLL.

Table 3-7 USB features

USB features	USB
Full speed mode	Yes
Configurable Endpoints	8
Independent SRAM	Yes
Dual-buffer mechanism	Yes
Wakeup/pending	Yes
Internal pull-up	Yes

3.33 AWU Timer

Device integrates an automatic wake-up timer (AWU). The AWU timer can count, and generate an interrupt to wake up the MCU from Stop mode and Standby mode.

3.34 Information Security

3.34.1 AES

HK32L08x/HK32L0Hx integrates an advanced encryption and decryption unit (AES), which follows FIPS197 (Federal Information Processing Standards).

- ECB mode
  - Key size: 128, 192 and 256 bits
  - Encrypting calculation time:
    - 128-bit key: 57 clock periods
    - 192-bit key: 67 clock periods
    - 256-bit key: 77 clock periods
  - Decrypting calculation time:
    - 128-bit key: 57 clock periods
    - 192-bit key: 67 clock periods
    - 256-bit key: 77 clock periods
- A 32-bit input buffer and a 32-bit output buffer
  - The buffer register access only supports 32-bit data width.
- Supports AES clock randomization, and cooperates with TRNG module to randomize AES clock.

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

- Interrupt field protection and interrupt field recovery
- Supports DMA (needs two DMA channels)

3.34.2 TRNG

HK32L08x/HK32L0Hx integrates a true random number generator (TRNG), based on a continuous analog noise, that provides a random 32-bit value to the host when read.

- 40 periods of the TRNG_CLK clock signals between two consecutive random numbers.
- Monitoring the TRNG entropy to flag abnormal behavior (generation of stable values, or of a stable sequence of values)
- It can be disabled to reduce power consumption
- The TRNG clock is divided by HSI.

3.35 96-bit UID

A 96-bit unique identification (UID) provides a reference number corresponding to each HK32L08x/HK32L0Hx SOC. In any circumstance, the ID is unique. You are prohibited to modify the UID. According to different applications, the 96-bit UID can be read in a unit of byte (8 bits), half-word (16 bits) or word (32 bits). The 96-bit UID is fit for the following applications:

- Used as a part number (for example, as a USB character list number or other terminal applications)
- Used as a keyword. When programming the Flash, use the UID with software encryption and decryption algorithms to improve security of the code in the Flash.
- To activate the boot process of the security mechanism.

3.36 Beeper

The beeper embeds an ultra-low power 7-bit timer. The clock of the timer can be configured to HSE, GPIO input clock or 128 kHz LSI. The counter counts down and outputs pulses at frequency of 1, 2, 4 or 8 kHz.

In Stop mode, the beeper continues to work and outputs pulses.

3.37 Debug Interface

Build-in ARM SWJ-DP interface, which combined with a single wire debug interface, to realize the connection between serial single wire debug interfaces (SWDIO and SWCLK).

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

4 Electrical characteristics

4.1 HK32L08x

4.1.1 Absolute maximum values

Note:

- *Stresses above the absolute maximum rating listed in Table 4-1 and Table 4-3 may cause permanent damage to the device.*
- *Exposure to maximum permitted conditions for extended periods may affect device reliability.*

4.1.1.1 Voltage characteristics

Table 4-1 Voltage characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})	-0.3	5.8	V
V_{IN}	Input voltage on pins	-0.3	5.8	
$\|V_{SSX} - V_{SS}\|$	Variation between different V_{DD} ground pins	-	50	mV

4.1.1.2 Current characteristics

Table 4-2 Current characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source) (1)	105	mA
I_{VSS}	Total current out of Vss ground lines (sink) (1)	105	
I_{IO}	Output current sunk by any I/O and control pin	16	
	Output current source by any I/O and control pin	16	
$I_{INJ(PIN)}$ (2)	Injected current on pins (3)	-5/+0	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pin) (4)	-25/+0	

(1). All main power (V_{DD}, V_{DDA}) and Ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

(2). Negative injected current disturbs the analog performance of the device.

(3). When $V_{IN} > V_{DD}$, a positive injected current is induced. When $V_{IN} < V_{SS}$, a negative injected current is induced, and the injected current must be limited to the permitted range.

(4). When several I/Os are submitted to a current injection, the maximum $\sum I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

4.1.1.3 Thermal characteristics

Table 4-3 Thermal characteristics

Symbol	Description	Min	Max	Unit
T_{STG}	Storage temperature range	-55	130	°C
T_J	Maximum junction temperature	-45	110	

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

4.1.2 Operation conditions

4.1.2.1 General operation conditions

Table 4-4 operation conditions

Symbol	Description	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	48	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	48	
f_{PCLK2}	Internal APB2 clock frequency	-	48	
V_{DD}	Standard operating voltage	1.8	4.2	V
V_{DDA}(1)	Analog operating voltage	1.8	4.2	V
T_A	Operating temperature	-40	85	℃

(1). V_{DDA} can less than V_{DD}, for example: V_{DD}=4.2V, V_{DDA}=3.3V; V_{DD}=3.3V, V_{DDA}=2.5V

4.1.2.2 PVD characteristics

Table 4-5 PVD characteristics

Symbol	Description	Conditions (-40℃ ~ 85℃)	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection (rising edge)	PLS[2:0]=000	1.84	1.92	2.01	V
		PLS[2:0]=001	2.00	2.12	2.20	
		PLS[2:0]=010	2.15	2.31	2.40	
		PLS[2:0]=011	2.35	2.50	2.60	
		PLS[2:0]=100	2.55	2.70	2.80	
		PLS[2:0]=101	2.70	2.87	2.98	
		PLS[2:0]=110	2.90	3.07	3.18	
	Programmable voltage detector level selection (falling edge)	PLS[2:0]=000	1.75	1.81	1.89	
		PLS[2:0]=001	1.90	2.00	2.09	
		PLS[2:0]=010	2.05	2.18	2.27	
		PLS[2:0]=011	2.20	2.36	2.47	
		PLS[2:0]=100	2.35	2.55	2.67	
		PLS[2:0]=101	2.50	2.72	2.83	
		PLS[2:0]=110	2.70	2.91	3.03	

4.1.2.3 BOR characteristics

Table 4-6 BOR characteristics

Symbol	Description	Conditions(-40 ~ 85℃)	Min	Typ	Max	Unit
V_{BOR}(1)	Brown-out reset threshold (The rising edge of V_{DD})	V_{BOR0}	1.68	1.73	1.78	V
		V_{BOR1}	1.70	1.83	1.92	
		V_{BOR2}	2.18	2.39	2.48	
		V_{BOR3}	2.36	2.58	2.68	
		V_{BOR4}	2.52	2.75	2.86	
	Brown-out reset threshold (The falling edge of V_{DD})	V_{BOR0}	1.58	1.63	1.69	
		V_{BOR1}	1.66	1.81	1.89	

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

Symbol	Description	Conditions(-40 ~ 85℃)	Min	Typ	Max	Unit
		V_{BOR2}	2.16	2.37	2.47	
		V_{BOR3}	2.34	2.56	2.65	
		V_{BOR4}	2.50	2.73	2.83	
t_{BORRST} (2)	Brown-out reset time	–	–	80	–	μs

(1). BOR only monitors V_{DD}。

(2). Guaranteed by design.

4.1.2.4 POR/PDR characteristics

Table 4-7 POR/PDR characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
$V_{POR/PDR}$ (1)	POR/PDR thresholds	Falling edge	1.49	1.65	1.78	V
		Rising edge	1.66	1.74	1.85	V
$V_{PDRhyst}$	PDR hysteresis	-	53	85	214	mV
$t_{RSTTEMPO}$ (2)	Reset time	-	-	2	-	ms

(1) POR/PDR only monitor V_{DD}.

(2) Design guarantees.

4.1.2.5 Embedded reference voltage

Table 4-8 Embedded reference voltage

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-40 - 85°C	-	1.2	-	V

4.1.2.6 Operating current

Table 4-9 Operating current characteristics

Mode	Conditions	Parameters	Temperature			Unit
			-40° C	25° C	85° C	
Run mode	HSI=8MHz, APB bus is on, V_{DD}=3.3V	Operating current	5.012	5.029	5.114	mA
	HSI=8MHz, APB bus is off, V_{DD}=3.3V		3.198	3.215	3.296	
	MSI=4.2MHz, APB bus is on, V_{DD}=3.3V		3.186	3.183	3.253	
	MSI=4.2MHz, APB bus is off, V_{DD}=3.3V		2.172	2.182	2.248	
	MSI=524KHz, APB bus is on, V_{DD}=3.3V		1.216	1.240	1.294	
	MSI=524KHz, APB bus is off, V_{DD}=3.3V		0.950	0.973	1.026	
Low-Power Run	LSI=32.768KHz, V_{DD} =3.3V	Operating current	8.41	8.78	17.29	μA
Sleep mode	LSI=32.768KHz, V_{DD} =3.3V	Operating current	197.75	201.36	243.67	μA
		Wakeup time	-	1.22	-	μs
Low-Power Sleep	LSI=32.768KHz V_{DD} =3.3V	Operating current	4.73	5.02	13.42	μA
		Wakeup time	-	1.29	-	μs
Stop	V_{DD} =3.3V	Operating current	44.24	52.42	71.87	μA

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

Mode	Conditions	Parameters	Temperature			Unit
			-40° C	25° C	85° C	
Mode		Wakeup time	-	2.98	-	μs
Low-Power Stop	V_{DD} =3.3V	Operating current	0.52	0.76	7.74	μA
		Wakeup time	-	9.55	-	μs
Standby Mode(1)	V_{DD} =3.3V	Operating current	0.15	0.24	2.08	μA
		Wakeup time	-	183	-	μs

(1). PDR is off.

4.1.2.7 High-speed external (HSE) RC oscillator

Table 4-10 HSE RC oscillator characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	24	MHz
R_F(1)	Feedback resistor	-	-	2	-	MΩ
$T_{su\ (HSE)}$(2)	Startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	2	-	ms
C	Recommended load reactance minus equivalent series capacitance of crystal oscillator (RS)		-	10	-	pF
$I_{DD\ (HSE)}$(1)	Power consumption	V_{DD}=3.3V, CL=10pF	-	140	-	μA

(1) Design guarantees.

(2) $T_{su\ (HSE)}$ represents the duration from the start time of HSE to the stable frequency output.

Device integrates a HSE RC oscillator circuitry with negative feedback. An oscillator circuit outside the chip is recommended as follows:

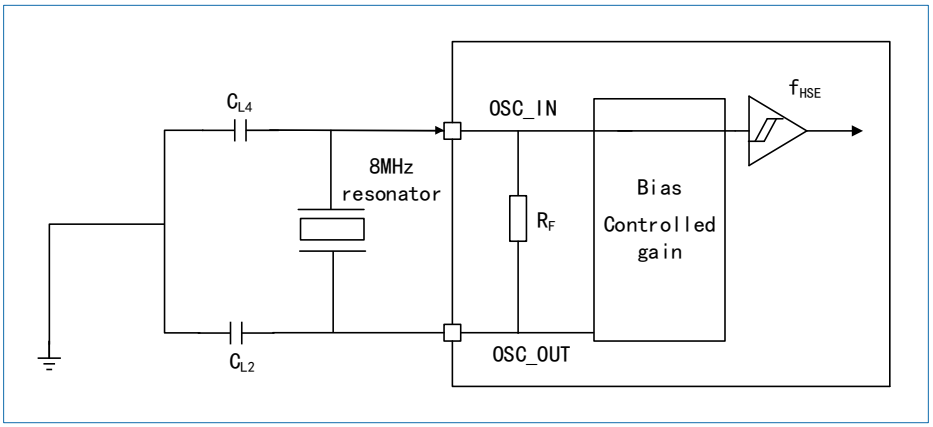


Figure 4-1 Typical application with HSE

HK32L08x can be clocked from the OSC_IN pin. The requirements of this clock signal are described as follows:

Table 4-11 HSE clock characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External clock source frequency	-	-	-	32	MHz
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

4.1.2.8 Low-speed external (LSE) RC oscillator

Table 4-12 LSE clock characteristics (f_{LSE}=32.768 kHz)

Symbol	Description	Conditions	Min	Typ	Max	Unit
R_F(1)	Feedback resistor	-	-	10	-	MΩ
$T_{su\ (LSE)}$(2)	Startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	1000	-	ms
C	Recommended load reactance minus equivalent series capacitance of crystal oscillator (RS)	-	-	10	-	pF
$I_{DD\ (LSE)}$(1)	Power consumption	V_{DD}=3.3V，CL=10pF	-	150	-	nA

(1) Design guarantees.

(2) $T_{su\ (LSE)}$ represents the duration from the start time of LSE to the stable frequency output.

HK32L08x integrates an LSE RC oscillator circuitry with negative feedback. An oscillator circuit outside the chip is recommended as follows:

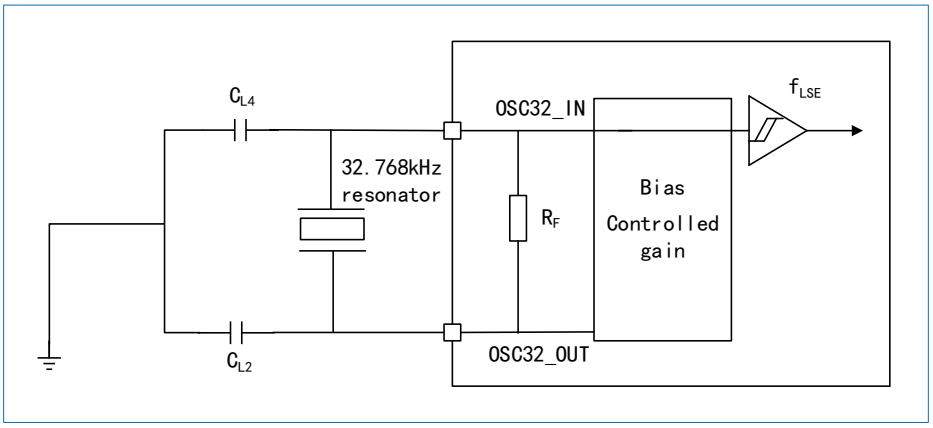


Figure 4-2 Typical application with LSE

HK32L08x can be clocked from the OSC32_IN pin. The requirements of this clock signal are described as follows:

Table 4-13 LSE clock characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	External clock source frequency	-	-	32.768	1000	kHz
$DuCy_{(LSE)}$	Duty cycle	-	45	-	55	%

(1) Design guarantees.

4.1.2.9 Middle-speed internal (MSI) RC oscillator

Table 4-14 MSIclock characteristics(1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{MSI}	Frequency (-40℃-85℃)	MSI range 0	255.95	262	264.48	kHz
		MSI range 1	510.08	524	528.49	
		MSI range 2	1.01	1.05	1.06	
		MSI range 3	2.01	2.1	2.16	
		MSI range 4	3.95	4.2	4.43	MHz
$DuCy_{(MSI)}$(1)	Duty cycle	-	45	-	55	%

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

$ACC_{(MSI)}$	Accuracy of the MSI oscillator	T_A= -40 - +85°C	-5	-	5	%
$T_{su\ (MSI)}$(1)	Startup time	MSI range 0	-	5	10	μs
$I_{DD\ (MSI)}$(1)	Power consumption (-40℃- 85℃)	MSI range 0	-	0.9	-	μA
		MSI range 1	-	1.5	-	
		MSI range 2	-	3.7	-	
		MSI range 3	-	6.2	-	
		MSI range 4	-	12.5	-	

(1) Design guarantees.

4.1.2.10 How-speed internal (HSI) RC oscillator

Table 4-15 HSI RC oscillator characteristics

Symbol	Description	Conditions		Min	Typ	Max	Unit
f_{HSI}(1)	Frequency	-		-	8	-	MHz
$DuCy_{(HSI)}$(1)	Duty cycle	-		45	-	55	%
$ACC_{(HSI)}$	Accuracy of the HSI oscillator	User-trimmed with the RCC_CR register		-1	-	1	
		Factory calibrated	T_A= –40 - +85°C	-0.86	-	1.27	%
			T_A= 0 - +70°C	0.5	-	1	
$T_{su\ (HSI)}$(1)	Startup time	$V_{SS} \le V_{IN} \le V_{DD}$		-	5	-	μs
$I_{DD\ (HSI)}$(1)	Power consumption	48MHz		-	68	87	μA

(1) Design guarantees.

4.1.2.11 Low-speed internal (LSI) RC oscillator

Table 4-16 LSI RC oscillator characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	31.451	32.768	34.022	kHz
$T_{su(LSI)}$ (1)	LSI oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	20	50	μs
$I_{DD(LSI)}$ (1)	LSI oscillator power consumption	-	-	450	750	μA

(1) Design guarantees.

4.1.2.12 PLL characteristics

Table 4-17 PLL characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max
f_{PLL_IN}	PLL input clock	2	-	80	MHz
	PLL input clock duty cycle	45	-	55	%
f_{PLL_OUT}	PLL multiplier output clock	25	-	48	MHz
t_{LOCK}	PLL lock time	-	50	75	us

(1) Design guarantees.

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

4.1.2.13 EEPROM characteristics

Table 4-18 EEPROM characteristics

Symbol	Description	Min	Typ	Max	Unit
T_{WRITE}	2K-bit programming time	-	-	5	ms
$I_{DDWRITE}$	Max current (SCL=400kHz)	-	0.3	0.5	mA
I_{DDREAD}	Max current (SCL=400kHz)	-	0.2	0.4	mA
N_{END}	Endurance	-	1000k	-	times
t_{RET}	Data retention	-	-	100	year

4.1.2.14 Flash memory characteristics

Table 4-19 Flash memory characteristics

Symbol	Description	Min	Typ	Max	Unit
T_{PROG}	A word programming time	6	-	7.5	μs
T_{ERASE}	Page erase time	4	-	5	ms
	Mass erase time	30	-	40	ms
I_{DDPROG}	programming current	-	-	4	mA
$I_{DDERASE}$	Page/mass erase time	-	-	2	mA
I_{DDREAD}	Supply current (read mode)	-	3.5mA@40MHz, 7uA@32KHz	4.5mA@40MHz, 2.5mA@5MHz for Margin1/0 read	mA
N_{END}	Endurance	100	-	-	kcycles
t_{RET}	Data retention	20	-	-	year

4.1.2.15 I/O port input characteristics

Table 4-20 I/O port statics characteristics(input)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	Input high level voltage	V_{DD}=3.3V	0.42*(V_{DD}-2V)+1V	-	V_{DD}	V
V_{IL}	Input low level voltage	V_{DD}=3.3V	-0.3	-	0.32*(V_{DD}-2V)+0.75V	V
V_{IHhys}	Input high level voltage	V_{DD}=3.3V	-	1.59	-	V
V_{ILhys}	Input low level voltage	V_{DD}=3.3V	-	1.44	-	V
V_{hys}	Schmitt trigger voltage hysteresis	V_{DD}=3.3V	-	150	-	mV
I_{lkg}	Input leakage current	V_{DD}=3.3V, 0<V_{IN}<3.3V	-	0.02	-	μA
		V_{DD}=3.3V, V_{IN}=5V	-	0.27	-	μA
R_{PU}	Pull-up resistor	V_{IN}=V_{SS}	30	40	50	KΩ
R_{PD}	Pull-down resistor	V_{IN}=V_{DD}	30	40	50	KΩ
C_{IO}(1)	I/O pin capacitance	-	-	5	-	pF

(1) Design guarantees.

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

4.1.2.16 I/O Output voltage characteristics

Table 4-21 I/O Output voltage characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{OH}	Output high level voltage	1.8 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-0.4	-	-	V
V_{OL}	Output low level voltage	1.8 V ≤ V_{DD} ≤ 3.6 V	-	-	0.4	V

Table 4-22 I/O output AC characteristics

Speed mode OSPEEDy[1:0]	Symbol	Description	Conditions	Min	Typ	Max	Unit
x0	$t_{f(IO)out}$	Output high to low level fall time	CL = 50 pF, V_{DD} = 3.3 V	62.9	77.1	91.2	ns
	$t_{r(IO)out}$	Output low to high level rise time		120.7	141	161.2	ns
01	$t_{f(IO)out}$	Output high to low level fall time	CL = 50 pF, V_{DD} = 3.3 V	5.5	8.2	10.8	ns
	$t_{r(IO)out}$	Output low to high level rise time		22.1	34.2	46.3	ns
11	$t_{f(IO)out}$	Output high to low level fall time	CL = 50 pF, V_{DD} = 3.3 V	3.5	3.9	4.3	ns
	$tr_{(IO)out}$	Output low to high level rise time		4.7	5.8	6.8	ns

4.1.2.17 NRST reset pin characteristics

NRST pin is integrated with inner a pull-up resistor, it can be connected with external RC circuit, or without any circuit.

Table 4-23 NRST pin input characteristics

Symbol	Description	Min	Tye	Max	Unit
T_{Noise}	Ignore time of low-level voltage	-	-	80	ns

4.1.2.18 TIM characteristics

Table 4-24 TIM characteristics

Symbol	Description	Min	Max	Unit
F_{EXT}	Timer external clock frequency on CH1 to CH4	-	$f_{TIMxCLK}/2$	MHz

(1). $f_{TIM\ x\ CLK}$ = 48 MHz

4.1.2.19 EMACC characteristics

Table 4-25 Motor drive frequency characteristics

System clock	ADC clock	Min	Tye	Max	Unit
48 MHz	$f_{PCLK} = f_{apb}$ $f_{ADC} = f_{PCLK}/4$	4	25	28	kHz

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

Table 4-26 EMACC and software efficiency compare when running FOC algorithms

Test conditions	electrical angle	Coordinate system transformation	SVPWM (software)	time	Unit
System clock: 48 MHz (Motor library with pure software)	14	13.03	7.56	34.59	μs
System clock: 48 MHz (Motor library with EMACC)	10	2.9	5.8	18.7	μs

4.1.2.20 ADC characteristics

Table 4-27 ADC characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DDA}	ADC power supply	-	1.8	3.3	4.2	V
VREFP	Positive reference voltage	-	1.8	-	V_{DDA}	V
VREFN	Negative reference voltage	-	0	0	0.1	V
f_{ADC}	ADC clock frequency	-	0.6	14	16.67	MHz
f_S (1)	Sampling frequency	f_{ADC} = 16 MHz	-	1	-	MHz
f_{TRIG} (1)	External trigger frequency	f_{ADC} = 16 MHz	-	-	941	kHz
			-	-	17	Cycles
V_{AIN}	Conversion voltage range	-	0	-	V_{REFP}	V
R_{AIN} (1)	External input impedance	Please refer to Table 4-28				kΩ
R_{ADC} (1)	Sampling switch resistance	-	-	0.3	6	kΩ
C_{ADC} (1)	Internal sample and hold capacitor	-	-	7	-	pF
$Jitter_{ADC}$	ADC trigger conversion jitter	-	-	1	-	Cycles
t_S (1)	Sampling rate	Continuous conversion	-	1.5	-	Cycles
t_{CONV} (1)	Total conversion time (including sampling time)	-	-	0.875	-	μs
		-	-	14	-	Cycles

(1) Design guarantees.

The max input impedance R_{AIN} must meet the following formula:

$$\mathbf{R}_{AIN} < \frac{\boldsymbol{Ts}}{\boldsymbol{f}_{ADC} \times \boldsymbol{C}_{ADC} \times \ln(2^{N+2})} - \boldsymbol{R}_{ADC}$$

N represents resolution, its value is 12.

Errors below 1/4 LSB (Least Significant Bit, LSB) is allowed.

Table 4-28 Max value of input impedance (f_{ADC} = 16 MHz)

Sampling period (Cycles)	Sampling time (t_S, μs)	Max input impedance (kΩ)
1.5	0.09	1.08
7.5	0.47	6.6
13.5	0.84	12.12
28.5	1.78	25.92
41.5	2.59	37.88
55.5	3.47	50.76
71.5	4.47	65.49

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

Sampling period (Cycles)	Sampling time (t_S, μs)	Max input impedance (kΩ)
239.5	14.97	220.06

Table 4-29 ADC resolution

Symbol	Parameter	Description	Conditions	Typ	Max	Unit
ET	Total unadjusted error (1)	maximum deviation between the actual and the idea transfer curves	V_{DD}=V_{DDA}=3.3V, f_{ADC} = 16 MHz, Measurements made after ADC calibration	-	3	LSB
EO	Offset error (2)	deviation between the first actual and the first idea transfer curves		-	2	
EG	Gain error (3)	-		-	1	
ED	Differential linearity error (4)	-		-	1	
EL	Integral linearity error (5)	-		-	1	

(1). Total unadjusted error: maximum deviation between the actual and the idea transfer curves.

(2). Offset error: deviation between the first actual and the first idea transfer curves.

(3). Gain error: deviation between the last actual and the last idea transfer curves.

(4). Differential linearity error: maximum deviation between actual steps and the idea one.

(5). Integral linearity error: maximum deviation between any actual transition and the end point correlation line.

Note:

- *ADC DC accuracy values are measured after internal calibration.*
- *ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.*
- *Better performance could be achieved in restricted VDD, frequency, VREF and temperature ranges.*
- *Based on characterization, not tested in production.*

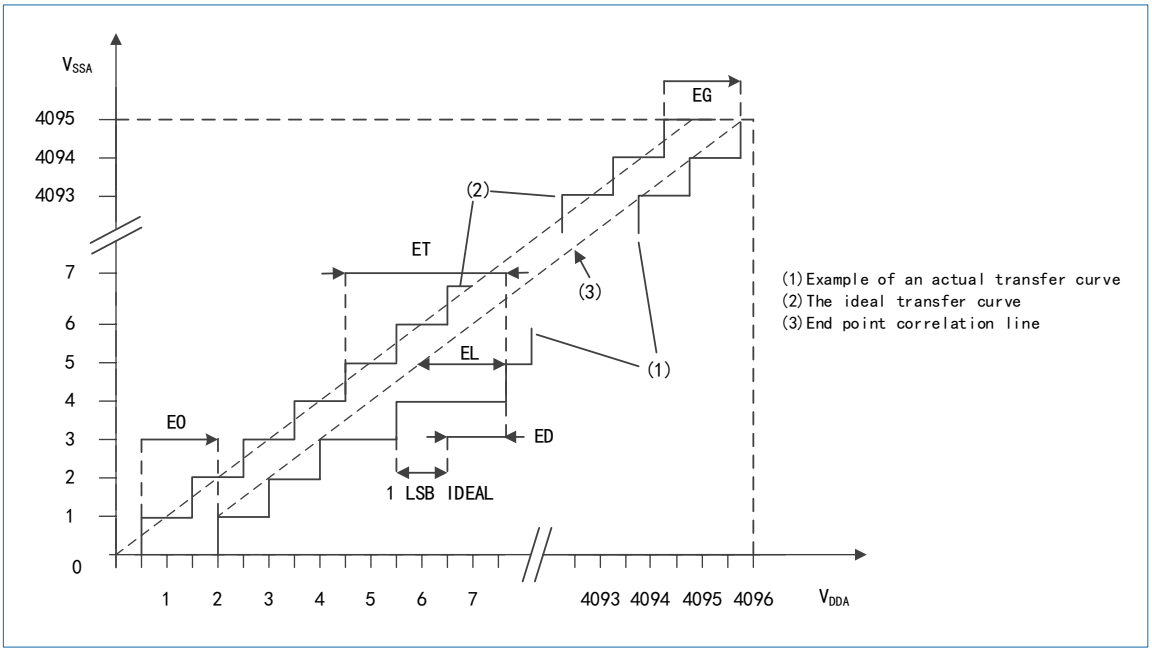


Figure 4-3 ADC accuracy characteristics

Note: Please refer to Table 4-29 for detail information of EO, ET, EG, EL, and ED.

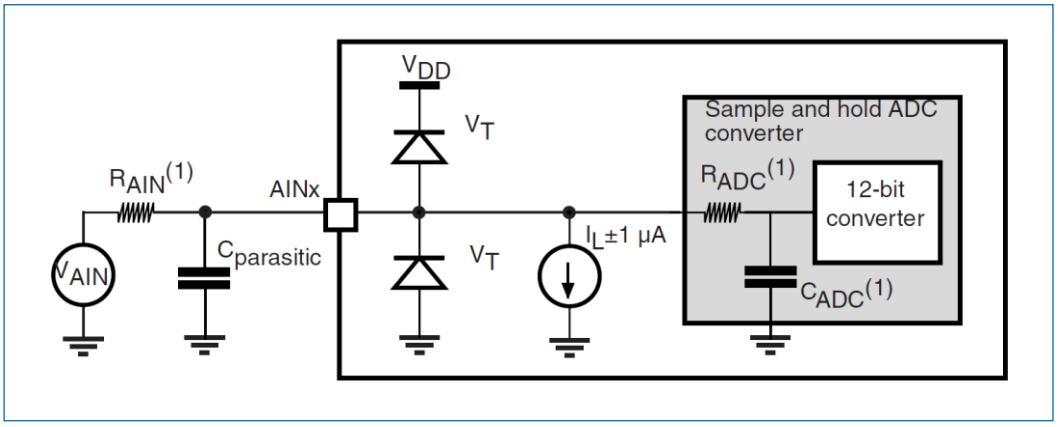


Figure 4-4 Typical connection diagram using the ADC

(1). Refer to Table 4-27 for the values of R_{ADC} and C_{ADC}.

$C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines:

Power supply decoupling should be performed as show in Figure 5-1. The 10 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

4.1.2.21 DAC characteristics

Table 4-30 DAC characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	3.3	4.2	V
INL	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	V_{DDA} = 3.3V	-2	-	2	LSB
DNL	Differential non linearity Difference between two consecutive code-1LSB	V_{DDA} = 3.3V	-2	-	2	LSB
Offset	Offset error (difference between measured value at Code (0x800) and the ideal value = VREF+/2)	V_{DDA} = 3.3V	-10	-	10	LSB
Gain error	Gain error	12-bit	-	-	4	LSB
R_O	Impedance output with buffer OFF	DAC buffer off	-	7	-	kΩ
C_{LOAD}(1)	Capacitive load	DAC buffer off	-	-	50	pF
t_{START}(1)	Start time	C_{LOAD} = 50 pF R_{LOAD} = 10kΩ	-	-	1	µs
$t_{DISABLE}$(1)	Disable time	C_{LOAD} = 50 pF R_{LOAD} = 10 kΩ	-	-	0.4	µs
I_{OUT}(1)	Output current	DAC buffer on	-	-	2	mA
I_{WORK}(1)	Operating current	DAC buffer off	-	1000	-	µA
		DAC buffer on	-	1500	-	
$I_{LEAKAGE}$(1)	Leakage current	DAC buffer off	-	30	-	nA

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

(1) Design guarantees.

4.1.2.22 Temperature sensor characteristics

Table 4-31 Temperature sensor characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
TL	V_{TS} linearity with temperature	-	-	-	±3	℃
V_{20}	Voltage at 20℃	20℃	845	924	990	mV
Avg_Slope	Average slope	-	-	2.85	-	mV/℃

4.1.2.23 Comparator characteristics

Table 4-32 COMP characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	3.3	4.2	V
Vcom	Common-mode input current	|VINP-VINN|≥30mV	0	-	V_{DDA}	V
Vdiff	Differential mode input voltage	VINP and VINN input range: 0 - V_{DDA}	30	-	-	mV
T_{start}(1)	Comparator startup time to reach propagation delay specification	-	-	1	7	μs
V_{hy}	Comparator hysteresis	No hysteresis	-	0	-	mV
		Low hysteresis	-	40	-	
		Medium hysteresis	-	80	-	
		High hysteresis	-	120	-	
I_{OP}	Comparator consumption from V_{DDA}	low-power mode	-	1	5	μA
		High-speed mode	-	5	12	
I_l(1)	Leakage current	Comparator is off	-	5	350	nA
T_{dly}(1)	Output delay (No hysteresis)	|VINP-VINN|≥30mV, High power mode, Rising edge	-	0.7	1	μs
		|VINP-VINN|≥30mV, low power mode , Rising edge	-	3	4	
		|VINP-VINN|≥30mV High power mode, falling edge	-	1.1	2.1	
		|VINP-VINN|≥30mV low power mode , falling edge	-	5.5	9.5	

(1) Design guarantees.

4.1.2.24 Operational amplifiers characteristics

Table 4-33 OPAMP characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	2	3.3	4.2	V
V_{OUT}	Output voltage	-	0.2	-	V_{DDA}-0.2	V

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

Symbol	Description	Conditions	Min	Typ	Max	Unit
CMIR	Common mode input range	-	0	-	V_{DDA}	V
I_{bias}(1)	Input offset current	-	-	1	-	μA
I_{load}	Output current	-	-	-	500	μA
I_q	Operating current	No load, static mode	-	1200	-	μA
I_l(1)	Leakage current	OPAMP off	-	5	-	nA
V_{OS}	Input offset voltage	Before calibration	-	±5	-	mV
		After calibration	-	±1.6	-	
CMRR	Common mode rejection ratio	-	-	90	-	dB
PSRR	Power supply rejection ratio	-	-	90	-	dB
GBW	Gain Bandwidth Product	-	6	8	-	MHz
SR	Slew rate	-	-	3.9	-	V/μs
ϕ	Phase margin	-	-	60	-	Deg
R_{load}(1)	Resistive load	-	4	-	-	kΩ
C_{load}(1)	Capacitive load	-	-	-	50	pF
PGA gain	PGA gain	Level 1	-	2	-	times
		Level 2	-	4	-	
		Level 3	-	8	-	
		Level 4	-	16	-	

(1) Design guarantees.

4.1.2.25 LCD controller characteristics

Table 4-34 LCD controller characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{LCD}	LCD power supply	-	2.6	-	3.6	V
V_{LCDx}(1)	V_{LCD0}	-	-	2.6	-	V
	V_{LCD1}		-	2.73	-	
	V_{LCD2}		-	2.86	-	
	V_{LCD3}		-	2.98	-	
	V_{LCD4}		-	3.12	-	
	V_{LCD5}		-	3.26	-	
	V_{LCD6}		-	3.4	-	
	V_{LCD7}		-	3.55	-	
C_{ext}	V_{LCD} external capacitance	-	0.1	-	2	uF
VREF(1)	Bandgap voltage reference	-	-	1.22	-	V
I_{BIAS}(1)	Reference current	-	-	0.18	-	uA

(1) Design guarantees.

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

4.2 HK32L0Hx

4.2.1 Absolute maximum values

Note:

- *Stresses above the absolute maximum rating listed in Table 4-35 and Table 4-37 may cause permanent damage to the device.*
- *Exposure to maximum permitted conditions for extended periods may affect device reliability.*

4.2.1.1 Voltage characteristics

Table 4-35 Voltage characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})	-0.3	5.8	V
V_{IN}	Input voltage on pins	-0.3	5.8	
$\|V_{SSX} - V_{SS}\|$	Variation between different V_{DD} ground pins	-	50	mV

4.2.1.2 Current characteristics

Table 4-36 Current characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source) (1)	105	mA
I_{VSS}	Total current out of Vss ground lines (sink) (1)	105	
I_{IO}	Output current sunk by any I/O and control pin	16	
	Output current source by any I/O and control pin	16	
$I_{INJ(PIN)}$ (2)	Injected current on pins (3)	-5/+0	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pin) (4)	-25/+0	

(5). All main power (V_{DD}, V_{DDA}) and Ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

(6). Negative injected current disturbs the analog performance of the device.

(7). When $V_{IN} > V_{DD}$, a positive injected current is induced. When $V_{IN} < V_{SS}$, a negative injected current is induced, and the injected current must be limited to the permitted range.

(8). When several I/Os are submitted to a current injection, the maximum $\sum I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

4.2.1.3 Thermal characteristics

Table 4-37 Thermal characteristics

Symbol	Description	Min	Max	Unit
T_{STG}	Storage temperature range	-55	130	℃
T_J	Maximum junction temperature	-45	110	

4.2.2 Operation conditions

4.2.2.1 General operation conditions

Table 4-38 operation conditions

Symbol	Description	Min	Max	Unit

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

f_{HCLK}	Internal AHB clock frequency	-	48	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	48	
f_{PCLK2}	Internal APB2 clock frequency	-	48	
V_{DD}	Standard operating voltage	2.7	5.5	V
V_{DDA}(1)	Analog operating voltage	2.7	5.5	V
T_A	Operating temperature	-40	85	℃

(2). V_{DDA} can less than V_{DD}, for example: V_{DD}=5V, V_{DDA}=4.2V, V_{DD}=3.3V, V_{DDA}=2.5V

4.2.2.2 PVD characteristics

Table 4-39 PVD characteristics

Symbol	Description	Conditions (-40℃ ~ 85℃)	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection (rising edge)	PLS[2:0]=101	2.70	2.87	2.98	V
		PLS[2:0]=110	2.90	3.07	3.18	
	Programmable voltage detector level selection (falling edge)	PLS[2:0]=101	2.50	2.72	2.83	
		PLS[2:0]=110	2.70	2.91	3.03	

4.2.2.3 BOR characteristics

Table 4-40 BOR characteristics

Symbol	Description	Conditions(-40 ~ 85℃)	Min	Typ	Max	Unit
V_{BOR}(1)	Brown-out reset threshold (The rising edge of V_{DD})	V_{BOR0}	2.18	2.39	2.48	V
		V_{BOR1}	2.36	2.58	2.68	
		V_{BOR2}	2.52	2.75	2.86	
	Brown-out reset threshold (The falling edge of V_{DD})	V_{BOR0}	2.16	2.37	2.47	
		V_{BOR1}	2.34	2.56	2.65	
		V_{BOR2}	2.50	2.73	2.83	
t_{BORRST}(2)	Brown-out reset time	–	–	80	–	μs

(3). BOR only monitors V_{DD}。

(4). Guaranteed by design.

4.2.2.4 POR/PDR characteristics

Table 4-41 POR/PDR characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
$V_{POR/PDR}$ (1)	POR/PDR thresholds	Falling edge	2.2	2.27	2.4	V
		Rising edge	2.26	2.35	2.5	V
$V_{PDRhyst}$	PDR hysteresis	-	62	79.5	105	mV
$t_{RSTTEMPO}$ (2)	Reset time	-	-	2	-	ms

(3) POR/PDR only monitor V_{DD}.

(4) Design guarantees.

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

4.2.2.5 Embedded reference voltage

Table 4-42 Embedded reference voltage

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-40 - 85°C	-	1.2	-	V

4.2.2.6 Operating current

Table 4-43 Operating current characteristics

Mode	Conditions	Parameters	Temperature			Unit
			-40° C	25° C	85° C	
Run mode	HSI=8MHz, APB bus is on, V_{DD}=3.3V	Operating current	5.012	5.029	5.114	mA
	HSI=8MHz, APB bus is off, V_{DD}=3.3V		3.198	3.215	3.296	
	MSI=4.2MHz, APB bus is on, V_{DD}=3.3V		3.186	3.183	3.253	
	MSI=4.2MHz, APB bus is off, V_{DD}=3.3V		2.172	2.182	2.248	
	MSI=524KHz, APB bus is on, V_{DD}=3.3V		1.216	1.240	1.294	
	MSI=524KHz, APB bus is off, V_{DD}=3.3V		0.950	0.973	1.026	
Low-Power Run	LSI=32.768KHz, V_{DD} =3.3V	Operating current	8.41	8.78	17.29	μA
Sleep mode	LSI=32.768KHz, V_{DD} =3.3V	Operating current	197.75	201.36	243.67	μA
		Wakeup time	-	1.22	-	μs
Low-Power Sleep	LSI=32.768KHz V_{DD} =3.3V	Operating current	4.73	5.02	13.42	μA
		Wakeup time	-	1.29	-	μs
Stop Mode	V_{DD} =3.3V	Operating current	44.24	52.42	71.87	μA
		Wakeup time	-	2.98	-	μs
Low-Power Stop	V_{DD} =3.3V	Operating current	0.52	0.76	7.74	μA
		Wakeup time	-	9.55	-	μs
Standby Mode(1)	V_{DD} =3.3V	Operating current	0.15	0.24	2.08	μA
		Wakeup time	-	183	-	μs

(1). PDR is off.

4.2.2.7 High-speed external (HSE) RC oscillator

Table 4-44 HSE RC oscillator characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	24	MHz
R_F(1)	Feedback resistor	-	-	2	-	MΩ
$T_{su\ (HSE)}$(2)	Startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	2	-	ms
C	Recommended load reactance minus equivalent series capacitance of crystal oscillator (RS)		-	10	-	pF
$I_{DD\ (HSE)}$(1)	Power consumption	V_{DD}=5V, CL=10pF	-	140	-	μA

(3) Design guarantees.

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

(4) Tsu (HSE) represents the duration from the start time of HSE to the stable frequency output.

Device integrates a HSE RC oscillator circuitry with negative feedback. An oscillator circuit outside the chip is recommended as follows:

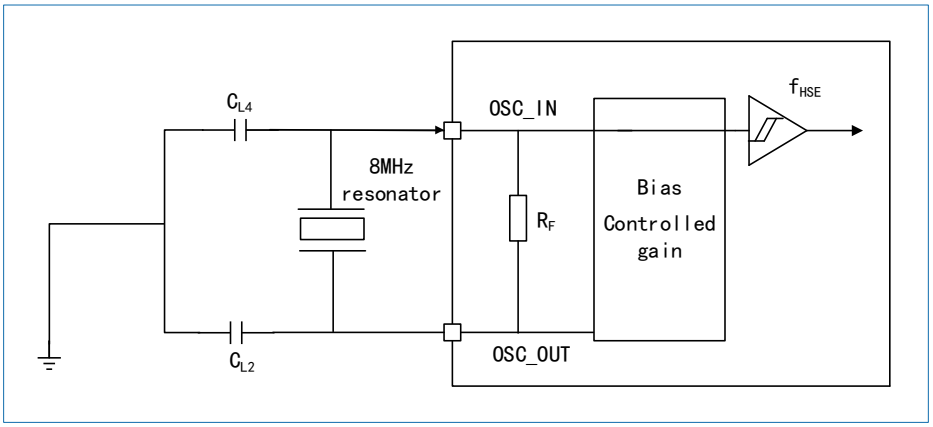


Figure 4-5 Typical application with HSE

HK32L0Hx can be clocked from the OSC_IN pin. The requirements of this clock signal are described as follows:

Table 4-45 HSE clock characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External clock source frequency	-	-	-	32	MHz
DuCy(HSE)	Duty cycle	-	45	-	55	%

4.2.2.8 Low-speed external (LSE) RC oscillator

Table 4-46 LSE clock characteristics (f_{LSE}=32.768 kHz)

Symbol	Description	Conditions	Min	Typ	Max	Unit
R_F(1)	Feedback resistor	-	-	10	-	MΩ
$T_{su\ (LSE)}$(2)	Startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	1000	-	ms
C	Recommended load reactance minus equivalent series capacitance of crystal oscillator (RS)	-	-	10	-	pF
$I_{DD\ (LSE)}$(1)	Power consumption	V_{DD}=5V，CL=10pF	-	150	-	nA

(1) Design guarantees.

(2) Tsu (LSE) represents the duration from the start time of LSE to the stable frequency output.

HK32L0Hx integrates an LSE RC oscillator circuitry with negative feedback. An oscillator circuit outside the chip is recommended as follows:

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

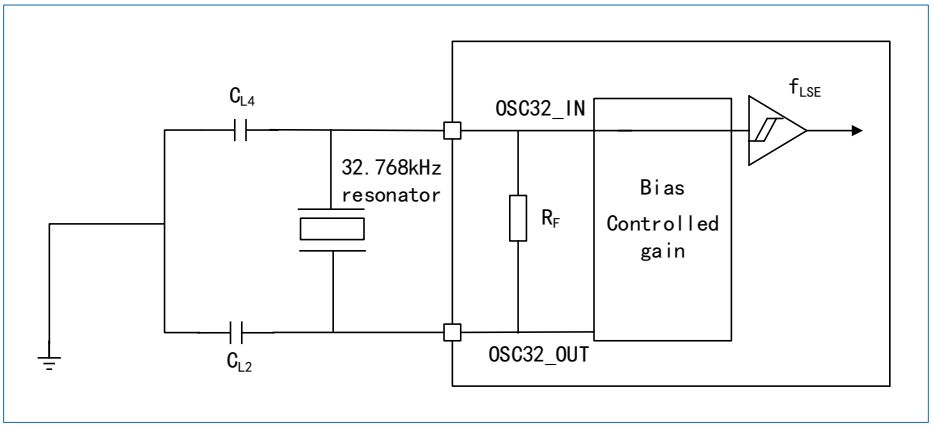


Figure 4-6 Typical application with LSE

HK32L0Hx can be clocked from the OSC32_IN pin. The requirements of this clock signal are described as follows:

Table 4-47 LSE clock characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	External clock source frequency	-	-	32.768	1000	kHz
$DuCy_{(LSE)}$	Duty cycle	-	45	-	55	%

(2) Design guarantees.

4.2.2.9 Middle-speed internal (MSI) RC oscillator

Table 4-48 MSI clock characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{MSI}	Frequency (-40℃- +85℃)	MSI range 0	255.95	262	264.48	kHz
		MSI range 1	510.08	524	528.49	
		MSI range 2	1.01	1.05	1.06	
		MSI range 3	2.01	2.1	2.16	
		MSI range 4	3.95	4.2	4.43	MHz
$DuCy_{(MSI)}$(1)	Duty cycle	-	45	-	55	%
$ACC_{(MSI)}$	Accuracy of the MSI oscillator	T_A= -40 - +85°C	-5	-	5	%
$T_{su\ (MSI)}$(1)	Startup time	MSI range 0	-	5	10	μs
$I_{DD\ (MSI)}$(1)	Power consumption (-40℃- 85℃)	MSI range 0	-	0.9	-	μA
		MSI range 1	-	1.5	-	
		MSI range 2	-	3.7	-	
		MSI range 3	-	6.2	-	
		MSI range 4	-	12.5	-	

(1) Design guarantees.

4.2.2.10 How-speed internal (HSI) RC oscillator

Table 4-49 HSI RC oscillator characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{HSI}(1)	Frequency	-	-	8	-	MHz
$DuCy_{(HSI)}$(1)	Duty cycle	-	45	-	55	%

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

Symbol	Description	Conditions		Min	Typ	Max	Unit
ACC (HSI)	Accuracy of the HSI oscillator	User-trimmed with the RCC_CR register		-1	-	1	
		Factory calibrated	T_A= –40 - +85°C	-0.86	-	1.27	%
			T_A= 0 - +70°C	0.5	-	1	
$T_{su\ (HSI)}$(1)	Startup time	$V_{SS} \le V_{IN} \le V_{DD}$		-	5	-	µs
$I_{DD\ (HSI)}$(1)	Power consumption	48MHz		-	68	87	µA

(1) Design guarantees.

4.2.2.11 Low-speed internal (LSI) RC oscillator

Table 4-50 LSI RC oscillator characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	31.451	32.768	34.022	kHz
$T_{su(LSI)}$ (1)	LSI oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	20	50	µs
$I_{DD(LSI)}$ (1)	LSI oscillator power consumption	-	-	450	750	µA

(1) Design guarantees.

4.2.2.12 PLL characteristics

Table 4-51 PLL characteristics (1)

Symbol	Description	Conditions	Min	Typ	Max
f_{PLL_IN}	PLL input clock	2	-	80	MHz
	PLL input clock duty cycle	45	-	55	%
f_{PLL_OUT}	PLL multiplier output clock	25	-	48	MHz
t_{LOCK}	PLL lock time	-	50	75	µs

(1) Design guarantees.

4.2.2.13 EEPROM characteristics

Table 4-52 EEPROM characteristics

Symbol	Description	Min	Typ	Max	Unit
T_{WRITE}	2K-bit programming time	-	-	5	ms
$I_{DDWRITE}$	Max current (SCL=400kHz)	-	0.3	0.5	mA
I_{DDREAD}	Max current (SCL=400kHz)	-	0.2	0.4	mA
N_{END}	Endurance	-	1000k	-	times
t_{RET}	Data retention	-	-	100	year

4.2.2.14 Flash memory characteristics

Table 4-53 Flash memory characteristics

Symbol	Description	Min	Typ	Max	Unit
T_{PROG}	A word programming time	6	-	7.5	µs
T_{ERASE}	Page erase time	4	-	5	ms
	Mass erase time	30	-	40	ms
I_{DDPROG}	programming current	-	-	4	mA

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

Symbol	Description	Min	Typ	Max	Unit
$I_{DDERASE}$	Page/mass erase time	-	-	2	mA
I_{DDREAD}	Supply current (read mode)	-	3.5mA@40MHz, 7uA@32KHz	4.5mA@40MHz, 2.5mA@5MHz for Margin1/0 read	mA
N_{END}	Endurance	100	-	-	kcycles
t_{RET}	Data retention	20	-	-	year

4.2.2.15 I/O port input characteristics

Table 4-54 I/O port statics characteristics(input)

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	Input high level voltage	V_{DD}=3.3V	0.42*(V_{DD}-2V)+1V	-	V_{DD}	V
V_{IL}	Input low level voltage	V_{DD}=3.3V	-0.3	-	0.32*(V_{DD}-2V)+0.75V	V
V_{IHhys}	Input high level voltage	V_{DD}=3.3V	-	2.52	-	V
V_{ILhys}	Input low level voltage	V_{DD}=3.3V	-	2.46	-	V
V_{hys}	Schmitt trigger voltage hysteresis	V_{DD}=3.3V	-	60	-	mV
I_{lkg}	Input leakage current	V_{DD}=3.3V, 0<V_{IN}<3.3V	-	0.02	-	μA
		V_{DD}=3.3V, V_{IN}=5V	-	0.27	-	μA
R_{PU}	Pull-up resistor	V_{IN}=V_{SS}	30	40	50	KΩ
R_{PD}	Pull-down resistor	V_{IN}=V_{DD}	30	40	50	KΩ
C_{IO}(1)	I/O pin capacitance	-	-	5	-	pF

(2) Design guarantees.

4.2.2.16 I/O Output voltage characteristics

Table 4-55 I/O Output voltage characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{OH}	Output high level voltage	1.8 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-0.4	-	-	V
V_{OL}	Output low level voltage	1.8 V ≤ V_{DD} ≤ 3.6 V	-	-	0.4	V

Table 4-56 I/O output AC characteristics

Speed mode OSPEEDy[1:0]	Symbol	Description	Conditions	Min	Typ	Max	Unit
x0	$t_{f(IO)out}$	Output high to low level fall time	CL = 50 pF, V_{DD} = 5 V	26.7	44.9	63.1	ns
	$t_{r(IO)out}$	Output low to high level rise time		61.7	92.1	122.5	ns
01	$t_{f(IO)out}$	Output high to low level fall time	CL = 50 pF, V_{DD} = 5 V	3.9	4.9	5.9	ns
	$t_{r(IO)out}$	Output low to high level rise time		7.3	14.1	20.9	ns
11	$t_{f(IO)out}$	Output high to low level fall time	CL = 50 pF, V_{DD} = 5 V	2.9	3.3	3.6	ns
	$tr_{(IO)out}$	Output low to high level rise time		3.7	4.4	5.1	ns

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

4.2.2.17 NRST reset pin characteristics

NRST pin is integrated with inner a pull-up resistor, it can be connected with external RC circuit, or without any circuit.

Table 4-57 NRST pin input characteristics

Symbol	Description	Min	Tye	Max	Unit
T_{Noise}	Ignore time of low-level voltage	-	-	80	ns

4.2.2.18 TIM characteristics

Table 4-58 TIM characteristics

Symbol	Description	Min	Max	Unit
F_{EXT}	Timer external clock frequency on CH1 to CH4	-	$f_{TIMxCLK}/2$	MHz

(2). $f_{TIM\ x\ CLK}$ = 48 MHz

4.2.2.19 EMACC characteristics

Table 4-59 Motor drive frequency characteristics

System clock	ADC clock	Min	Tye	Max	Unit
48 MHz	$f_{PCLK} = f_{APB}$ $f_{ADC} = f_{PCLK}/4$	4	25	28	kHz

Table 4-60 EMACC and software efficiency compare when running FOC algorithms

Test conditions	electrical angle	Coordinate system transformation	SVPWM (software)	time	Unit
System clock: 48 MHz (Motor library with pure software)	14	13.03	7.56	34.59	μs
System clock: 48 MHz (Motor library with EMACC)	10	2.9	5.8	18.7	μs

4.2.2.20 ADC characteristics

Table 4-61 ADC characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DDA}	ADC power supply	-	2.7	5	5.5	V
VREFP	Positive reference voltage	-	2.7	-	V_{DDA}	V
VREFN	Negative reference voltage	-	0	0	0.1	V
f_{ADC}	ADC clock frequency	-	0.6	14	16.67	MHz
f_S (1)	Sampling frequency	f_{ADC} = 16 MHz	-	1	-	MHz
f_{TRIG} (1)	External trigger frequency	f_{ADC} = 16 MHz	-	-	941	kHz
			-	-	17	Cycles
V_{AIN}	Conversion voltage range	-	0	-	V_{REFP}	V
R_{AIN} (1)	External input impedance	Please refer to Table 4-62				kΩ
R_{ADC} (1)	Sampling switch resistance	-	-	0.3	6	kΩ
C_{ADC} (1)	Internal sample and hold capacitor	-	-	7	-	pF

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

Symbol	Description	Conditions	Min	Typ	Max	Unit
$Jitter_{ADC}$	ADC trigger conversion jitter	-	-	1	-	Cycles
t_S (1)	Sampling rate	Continuous conversion	-	1.5	-	Cycles
t_{CONV} (1)	Total conversion time (including sampling time)	-	-	0.875	-	μs
		-	-	14	-	Cycles

(1) Design guarantees.

The max input impedance R_{AIN} must meet the following formula:

$$\mathbf{R}_{AIN} < \frac{\boldsymbol{Ts}}{\boldsymbol{f}_{ADC} \times \boldsymbol{C}_{ADC} \times \ln(2^{N+2})} - \boldsymbol{R}_{ADC}$$

N represents resolution, its value is 12.

Errors below 1/4 LSB (Least Significant Bit, LSB) is allowed.

Table 4-62 Max value of input impedance (f_{ADC} = 16 MHz)

Sampling period (Cycles)	Sampling time (t_S, μs)	Max input impedance (kΩ)
1.5	0.09	1.08
7.5	0.47	6.6
13.5	0.84	12.12
28.5	1.78	25.92
41.5	2.59	37.88
55.5	3.47	50.76
71.5	4.47	65.49
239.5	14.97	220.06

Table 4-63 ADC resolution

Symbol	Parameter	Description	Conditions	Typ	Max	Unit
ET	Total unadjusted error (1)	maximum deviation between the actual and the idea transfer curves	V_{DD}=V_{DDA}=3.3V, f_{ADC} = 16 MHz, Measurements made after ADC calibration	-	3	LSB
EO	Offset error (2)	deviation between the first actual and the first idea transfer curves		-	2	
EG	Gain error (3)	_		-	1	
ED	Differential linearity error (4)	_		-	1	
EL	Integral linearity error (5)	_		-	1	

(1). Total unadjusted error: maximum deviation between the actual and the idea transfer curves.

(2). Offset error: deviation between the first actual and the first idea transfer curves.

(3). Gain error: deviation between the last actual and the last idea transfer curves.

(4). Differential linearity error: maximum deviation between actual steps and the idea one.

(5). Integral linearity error: maximum deviation between any actual transition and the end point correlation line.

Note:

- *ADC DC accuracy values are measured after internal calibration.*

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

- *ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.*
- *Better performance could be achieved in restricted VDD, frequency, VREF and temperature ranges.*
- *Based on characterization, not tested in production.*

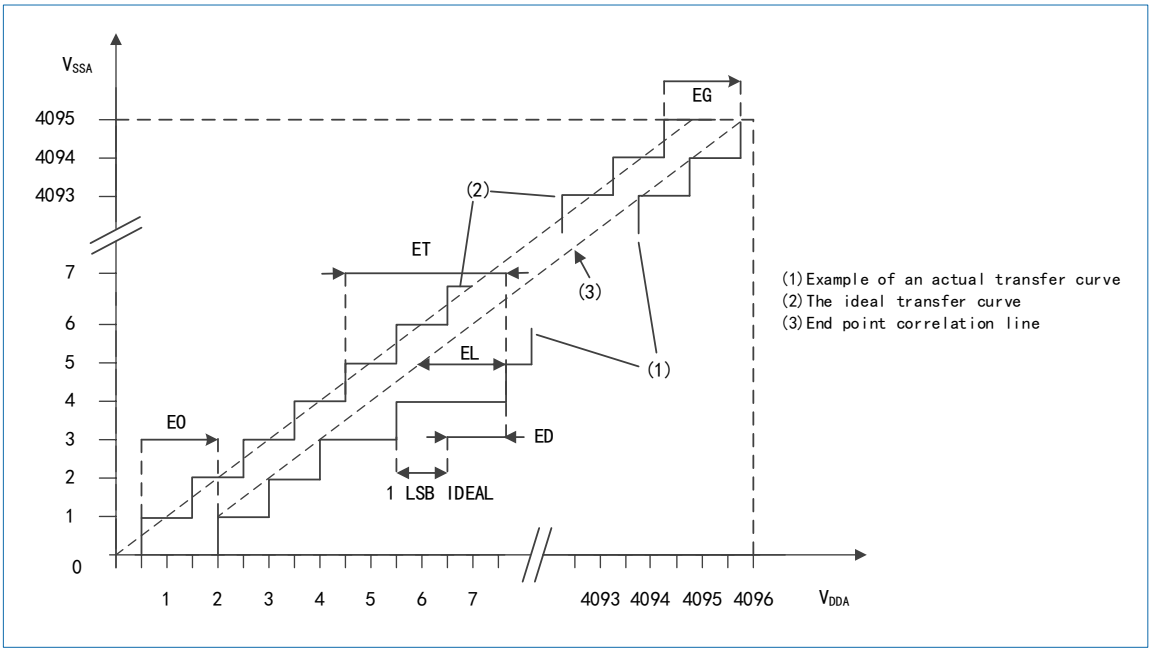


Figure 4-7 ADC accuracy characteristics

Note: Please refer to Table 4-63 for detail information of EO, ET, EG, EL, and ED.

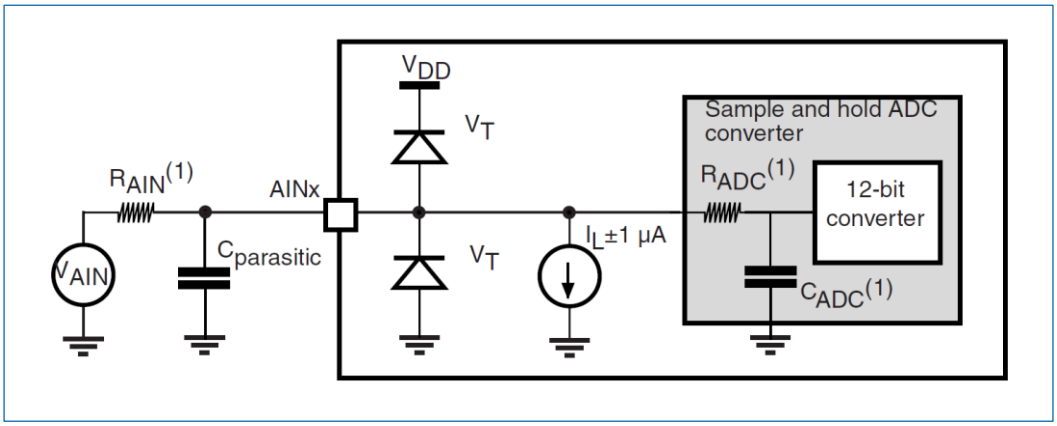


Figure 4-8 Typical connection diagram using the ADC

(1). Refer to Table 4-27 for the values of R_{ADC} and C_{ADC}.

$C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines:

Power supply decoupling should be performed as show in Figure 5-1. The 10 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

4.2.2.21 DAC characteristics

Table 4-64 DAC characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	2.7	5	5.5	V
INL	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	V_{DDA} = 5V	-2	-	2	LSB
DNL	Differential non linearity Difference between two consecutive code-1LSB	V_{DDA} = 5V	-2	-	2	LSB
Offset	Offset error (difference between measured value at Code (0x800) and the ideal value = VREF+/2)	V_{DDA} = 5V	-10	-	10	LSB
Gain error	Gain error	12-bit	-	-	4	LSB
R_O	Impedance output with buffer OFF	DAC buffer off	-	7	-	kΩ
C_{LOAD}(1)	Capacitive load	DAC buffer off	-	-	50	pF
t_{START}(1)	Start time	C_{LOAD} = 50 pF R_{LOAD} = 10kΩ	-	-	1	µs
$t_{DISABLE}$(1)	Disable time	C_{LOAD} = 50 pF R_{LOAD} = 10 kΩ	-	-	0.4	µs
I_{OUT}(1)	Output current	DAC buffer on	-	-	2	mA
I_{WORK}(1)	Operating current	DAC buffer off	-	1000	-	µA
		DAC buffer on	-	1500	-	
$I_{LEAKAGE}$(1)	Leakage current	DAC buffer off	-	30	-	nA

(1) Design guarantees.

4.2.2.22 Temperature sensor characteristics

Table 4-65 Temperature sensor characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
TL	V_{TS} linearity with temperature	-	-	-	±3	℃
V_{20}	Voltage at 20℃	20℃	845	924	990	mV
Avg_Slope	Average slope	-	-	2.85	-	mV/℃

4.2.2.23 Comparator characteristics

Table 4-66 COMP characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	2.7	5	5.5	V
Vcom	Common-mode input current	|VINP-VINN|≥30mV	0	-	V_{DDA}	V
Vdiff	Differential mode input voltage	VINP and VINN input range: 0 - V_{DDA}	30	-	-	mV
T_{start}(1)	Comparator startup time to reach propagation delay specification	-	-	1	7	µs
V_{hy}	Comparator hysteresis	No hysteresis	-	0	-	mV

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

Symbol	Description	Conditions	Min	Typ	Max	Unit
		Low hysteresis	-	40	-	
		Medium hysteresis	-	80	-	
		High hysteresis	-	120	-	
I_{OP}	Comparator consumption from V_{DDA}	low-power mode	-	1	5	μA
		High-speed mode	-	5	12	
I_l(1)	Leakage current	Comparator is off	-	5	350	nA
T_{dly}(1)	Output delay (No hysteresis)	|VINP-VINN|≥30mV, High power mode, Rising edge	-	0.7	1	μs
		|VINP-VINN|≥30mV, low power mode , Rising edge	-	3	4	
		|VINP-VINN|≥30mV High power mode, falling edge	-	1.1	2.1	
		|VINP-VINN|≥30mV low power mode , falling edge	-	5.5	9.5	

(1) Design guarantees.

4.2.2.24 Operational amplifiers characteristics

Table 4-67 OPAMP characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	2.7	5	5.5	V
V_{OUT}	Output voltage	-	0.2	-	V_{DDA}-0.2	V
CMIR	Common mode input range	-	0	-	V_{DDA}	V
I_{bias}(1)	Input offset current	-	-	1	-	uA
I_{load}	Output current	-	-	-	500	uA
I_q	Operating current	No load, static mode	-	1200	-	uA
I_l(1)	Leakage current	OPAMP off	-	5	-	nA
V_{OS}	Input offset voltage	Before calibration	-	±5	-	mV
		After calibration	-	±1.6	-	
CMRR	Common mode rejection ratio	-	-	90	-	dB
PSRR	Power supply rejection ratio	-	-	90	-	dB
GBW	Gain Bandwidth Product	-	6	8	-	MHz
SR	Slew rate	-	-	3.9	-	V/μs
ϕ	Phase margin	-	-	60	-	Deg
R_{load}(1)	Resistive load	-	4	-	-	kΩ
C_{load}(1)	Capacitive load	-	-	-	50	pF
PGA gain	PGA gain	Level 1	-	2	-	times
		Level 2	-	4	-	

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

Symbol	Description	Conditions	Min	Typ	Max	Unit
		Level 3	-	8	-	
		Level 4	-	16	-	

(1) Design guarantees.

4.2.2.25 LCD controller characteristics

Table 4-68 LCD controller characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{LCD}	LCD power supply	-	2.6	-	3.6	V
V_{LCDx}(1)	V_{LCD0}	-	-	2.6	-	V
	V_{LCD1}		-	2.73	-	
	V_{LCD2}		-	2.86	-	
	V_{LCD3}		-	2.98	-	
	V_{LCD4}		-	3.12	-	
	V_{LCD5}		-	3.26	-	
	V_{LCD6}		-	3.4	-	
	V_{LCD7}		-	3.55	-	
C_{ext}	V_{LCD} external capacitance	-	0.1	-	2	uF
VREF(1)	Bandgap voltage reference	-	-	1.22	-	V
I_{BIAS}(1)	Reference current	-	-	0.18	-	uA

(1) Design guarantees.

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

5 Typical circuitry

5.1 Power supply scheme

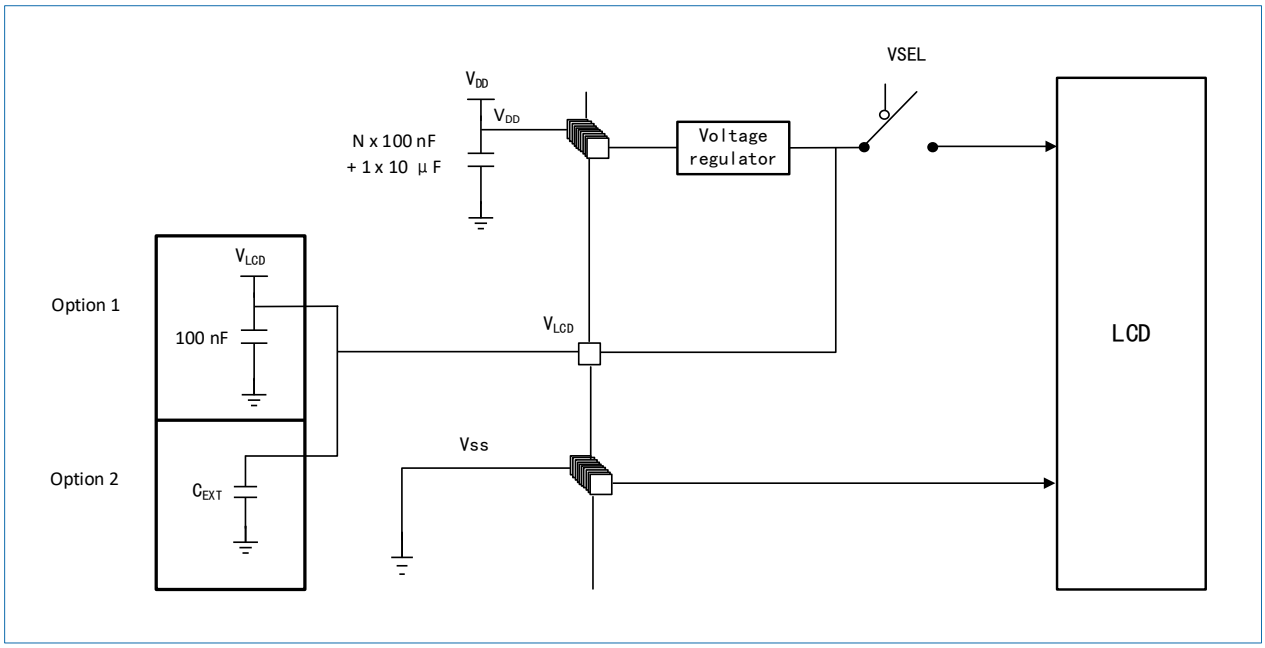


Figure 5-1 Power Supply scheme

6 Pinouts and pin descriptions

HK32L08x/HK32L0Hx provides the packages below.

6.1 LQFP64

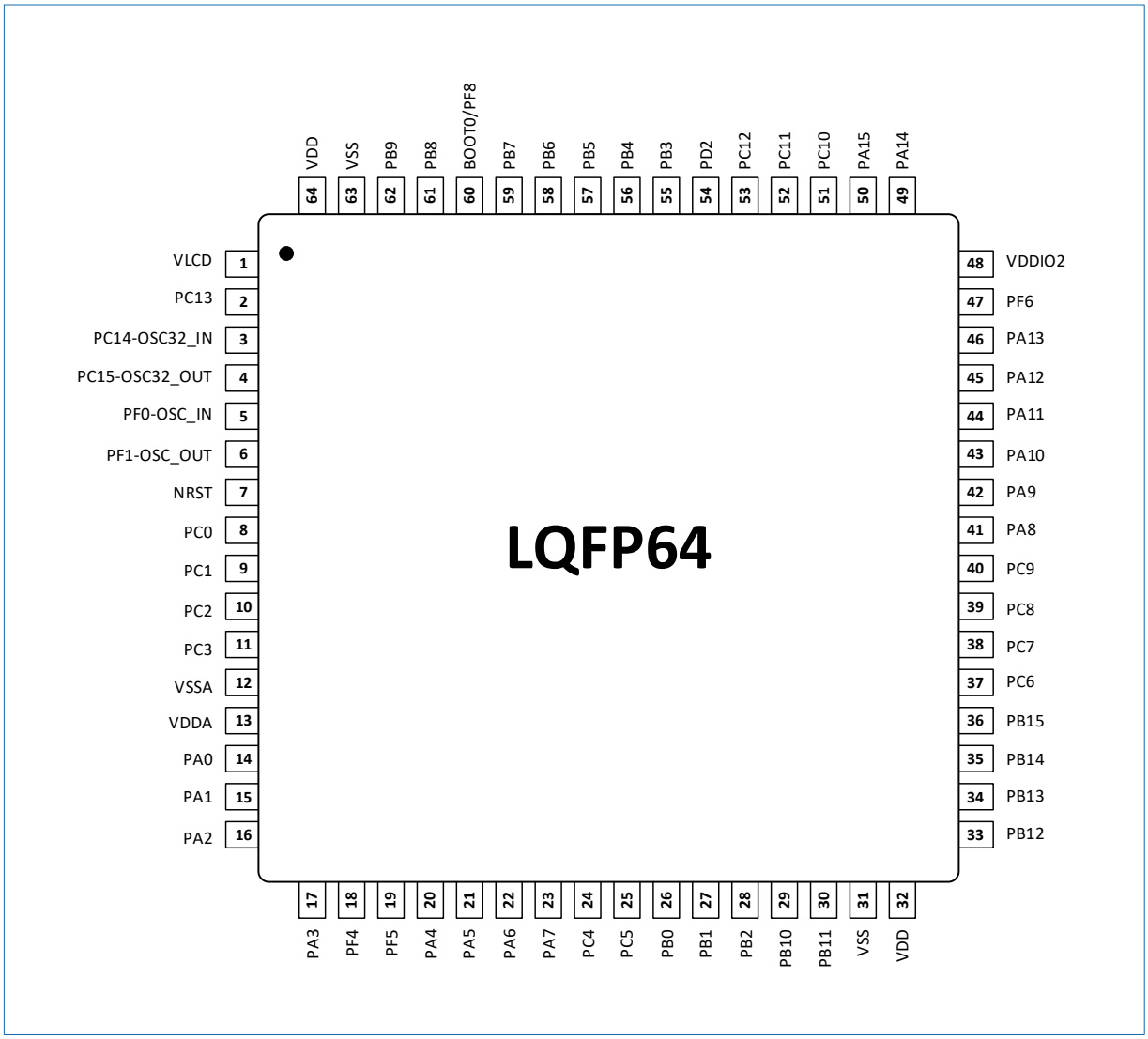


Figure 6-1 LQFP64 package pinout

6.2 LQFP48

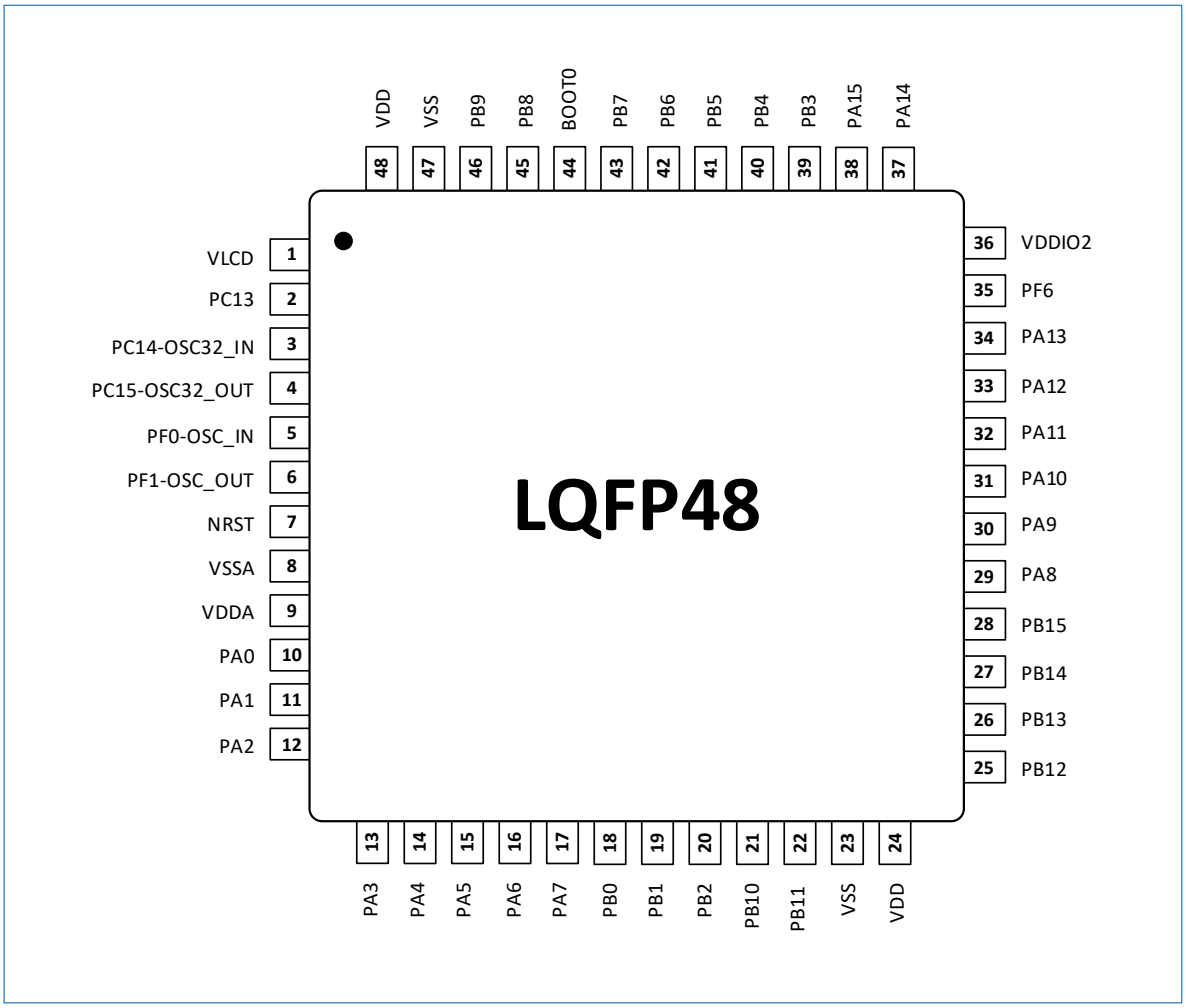


Figure 6-2 LQFP48 package pinout

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

6.3 LQFP32

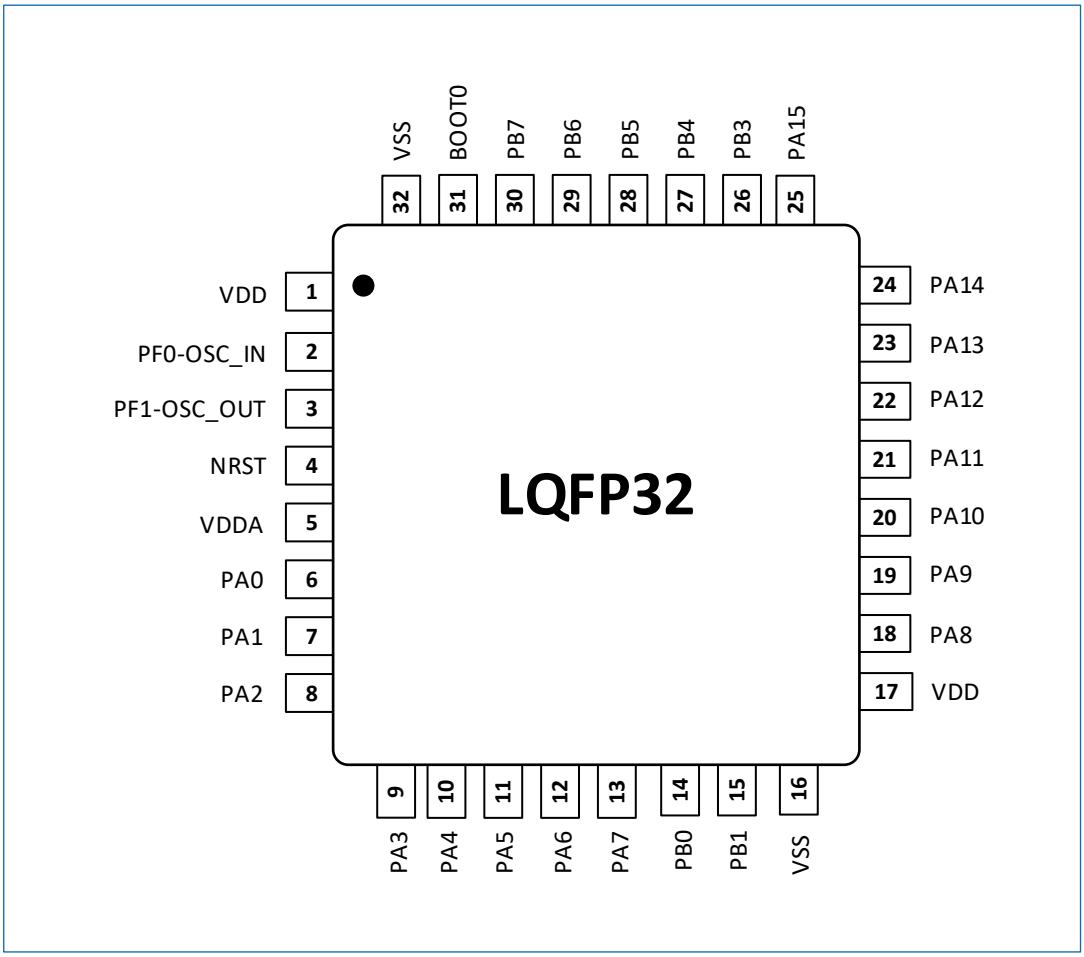


Figure 6-3 LQFP32 package pinout

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

6.4 QFN32

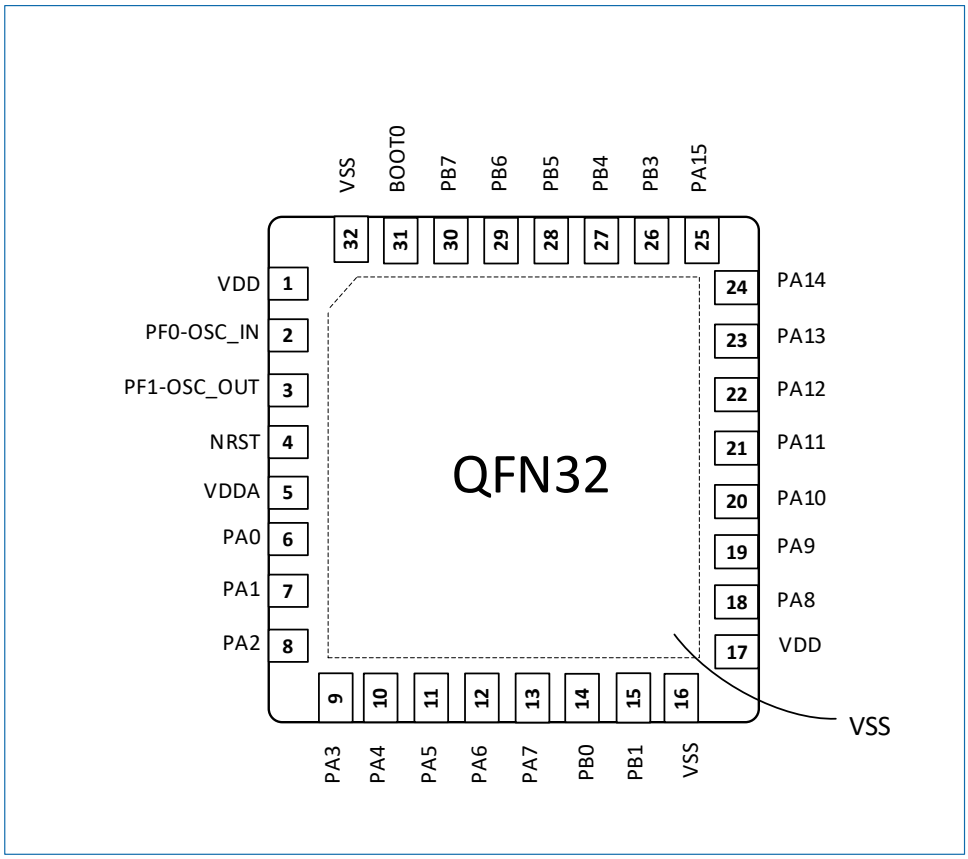


Figure 6-4 QFN32 package pinout

6.5 QFN28

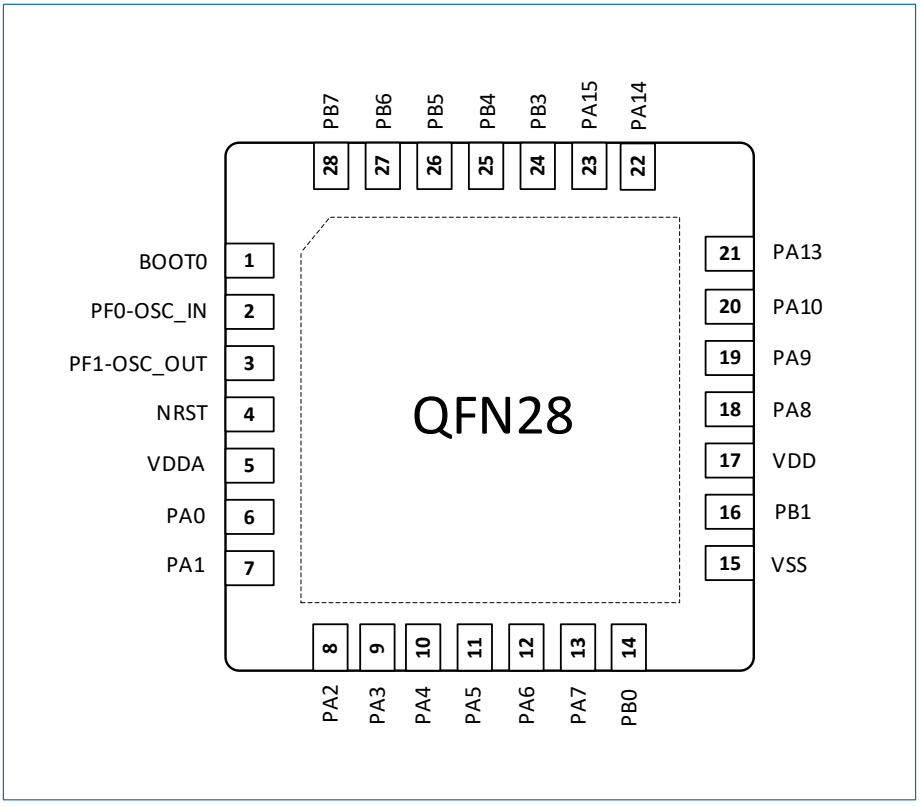


Figure 6-5 QFN28 package pinout

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

6.6 TSSOP20

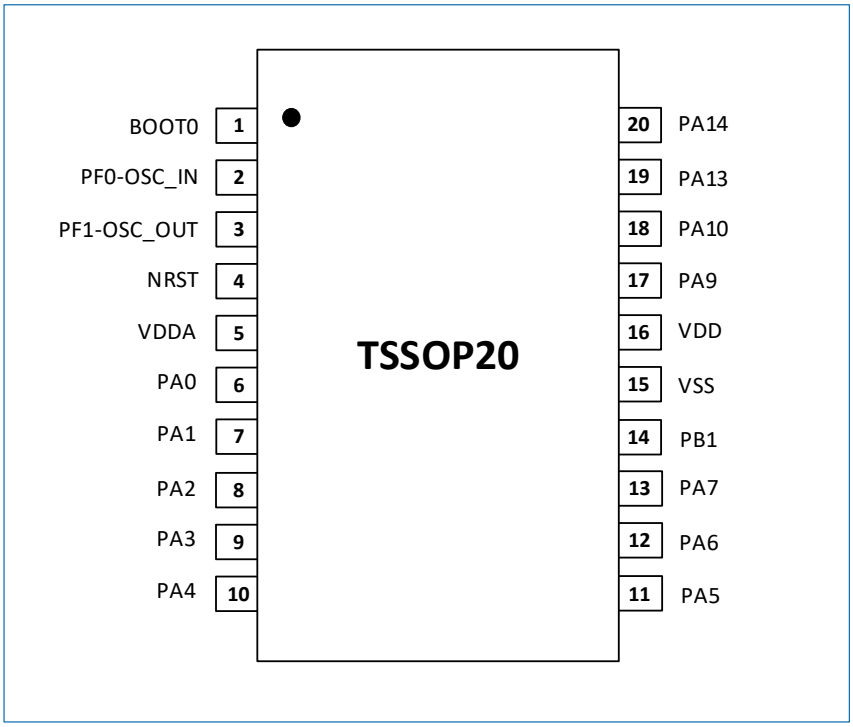


Figure 6-6 TSSOP20 package pinout

6.7 Pin definition

Table 6-1 HK32L08x/HK32L0Hx Pin Alternate functions

Pin number						Pin Name (Function after reset)	Pin type (1)	5V tolerant	Pin functions	
LQFP64	LQFP48	LQFP32	QFN32	QFN28	TSSOP20				Alternate functions	Additional functions
1	1	-	-	-	-	VLCD	S		LCD Power Supply	
2	2	-	-	-	-	PC13	I/O	FT	-	RTC_TAMP1/RTC_TS/ RTC_OUT WKUP2 EXTI13
3	3	-	-	-	-	PC14	I/O		-	OSC32_IN LSE_CKI EXTI14
4	4	-	-	-	-	PC15	I/O		-	OSC32_OUT EXTI15
5	5	2	2	2	2	PF0	I/O		I2C1_SDA	OSC_IN HSE_CKI EXTI0
6	6	3	3	3	3	PF1	I/O		I2C1_SCL	OSC_OUT EXTI1
7	7	4	4	4	4	NRST	I/O		-	NRST
8	-	-	-	-	-	PC0	I/O	FT	EVENTOUT LPTIM1_IN1	ADC_10 LCD_SEG18 EXTI0
9	-	-	-	-	-	PC1	I/O	FT	EVENTOUT LPTIM1_OUT	ADC_11 LCD_SEG19 EXTI1
10	-	-	-	-	-	PC2	I/O	FT	EVENTOUT SPI2_MISO/ I2S2_MCK	ADC_12 LCD_SEG20 EXTI2

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

Pin number						Pin Name (Function after reset)	Pin type (1)	5V tolerant	Pin functions	
LQFP64	LQFP48	LQFP32	QFN32	QFN28	TSSOP20				Alternate functions	Additional functions
									LPTIM1_IN2	
11	-	-	-	-	-	PC3	I/O	FT	EVENTOUT SPI2_MOSI/ I2S2_SD LPTIM1_ETR	ADC_13/ADC_19_BUF LCD_SEG21 EXTI3
12	8	-	-	-	-	VSSA	S		Analog ground	
13	9	5	5	5	5	VDDA	S		Analog Power Supply	
14	10	6	6	6	6	PA0	I/O	FT	USART1_CTS USART2_CTS TIM2_CH1/TIM2_ETR COMP1_OUT LPTIM3_IN1 UART4_TX	ADC_0 WKUP1 VREF2_OUT COMP1_IN1- TAMP2 EXTI0
15	11	7	7	7	7	PA1	I/O	FT	USART1_RTS/ USART1_DE USART2_RTS/ USART2_DE UART4_RX EVENTOUT TIM15_CH1N TIM2_CH2 LPTIM3_OUT	ADC_1 LCD_SEG0 COMP1_IN0+ OAMP1_IN3+ OAMP3_IN2+ EXTI1
16	12	8	8	8	8	PA2	I/O	FT	USART1_TX USART2_TX TIM15_CH1 TIM2_CH3 COMP2_OUT LPTIM3_IN2	ADC_2 LCD_SEG1 COMP2_IN VREF_TEST EXTI2
17	13	9	9	9	9	PA3	I/O	FT	USART1_RX USART2_RX TIM15_CH2 TIM2_CH4 LPTIM3_ETR	ADC_3 LCD_SEG2 EXTI3 COMP2_IN0+ OAMP1_IN2+ OAMP1_IN1- T_Sensor_OUT EXTI3
18	-	-	-	-	-	PF4	I/O	FT	EVENTOUT BEEPER CLU0_O CLU1_O CLU2_O CLU3_O	EXTI4
19	-	-	-	-	-	PF5	I/O		EVENTOUT BEEPER CLU0_O CLU1_O CLU2_O CLU3_O	OAMP3_OUT EXTI5
20	14	10	10	10	10	PA4	I/O		USART1_CK USART2_CK UART3_TX TIM14_CH1 LPTIM2_IN1 SPI1_NSS/I2S1_WS	ADC_4 DAC_OUT CKI_1 COMP1_IN2 COMP2_IN2 OAMP1_IN1+ OAMP2_IN0+ OAMP3_IN0+ EXTI4
21	15	11	11	11	11	PA5	I/O		UART3_RX	ADC_5

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

Pin number						Pin Name (Function after reset)	Pin type (1)	5V tolerant	Pin functions	
LQFP64	LQFP48	LQFP32	QFN32	QFN28	TSSOP20				Alternate functions	Additional functions
									TIM2_CH1/TIM2_ETR LPTIM2_OUT SPI1_SCK/I2S1_CK	COMP1_IN3- COMP2_IN3- OAMP1_OUT OAMP2_IN1- OAMP3_IN1+ EXTI5
22	16	12	12	12	12	PA6	I/O	FT	EVENTOUT CAN_RX UART3_CTS UART4_CTS LPUART1_CTS TIM1_BKIN TIM3_CH1 TIM16_CH1 LPTIM2_IN2 SPI1_MISO/I2S1_MCK COMP1_OUT	ADC_6 LCD_SEG3 EXTI6
23	17	13	13	13	13	PA7	I/O	FT	MCO EVENTOUT CAN_TX UART3_RTS/UART3_DE TIM1_CH1N TIM3_CH2 TIM14_CH1 TIM17_CH1 LPTIM2_ETR SPI1_MOSI/I2S1_SD COMP2_OUT BEEPER	ADC_7 LCD_SEG4 OAMP1_IN0+ OAMP2_IN3+ EXTI7
24	-	-	-	-	-	PC4	I/O	FT	UART3_TX UART4_TX EVENTOUT LPUART1_TX	ADC_14 LCD_SEG22 EXTI4
25	-	-	-	-	-	PC5	I/O	FT	UART3_RX UART4_RX LPUART1_RX	ADC_15 LCD_SEG23 OAMP1_IN0- OAMP2_IN0- EXTI5
26	18	14	14	14	-	PB0	I/O	FT	EVENTOUT TIM1_CH2N TIM3_CH3 BEEPER CLU0_O CLU1_O CLU2_O CLU3_O	ADC_8 LCD_SEG5 LCD_VLCD3 VREF0_OUT OAMP2_IN2+ OAMP3_IN3+ EXTI0
27	19	15	15	15	14	PB1	I/O	FT	UART3_RTS/UART3_DE UART4_RTS/UART4_DE LPUART1_RTS/LPUART1_DE TIM1_CH3N TIM3_CH4 TIM14_CH1 LPTIM3_OUT BEEPER CLU0_O CLU1_O CLU2_O CLU3_O	ADC_9 LCD_SEG6 VREF1_OUT EXTI1

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

Pin number						Pin Name (Function after reset)	Pin type (1)	5V tolerant	Pin functions	
LQFP64	LQFP48	LQFP32	QFN32	QFN28	TSSOP20				Alternate functions	Additional functions
28	20	-		-	-	PB2	I/O		I2C1_SMBA I2C2_SMBA LPTIM1_OUT	LCD_VLCD2 OAMP2_OUT OAMP3_IN1- EXTI2
29	21	-	-	-	-	PB10	I/O	FT	I2C1_SCL I2C2_SCL UART3_TX UART4_TX LPUART1_TX TIM2_CH3 SPI2_SCK/I2S2_CK	LCD_SEG10 OAMP3_IN0- EXTI10
30	22	-	-	-	-	PB11	I/O	FT	EVENTOUT I2C1_SDA I2C2_SDA UART3_RX UART4_RX LPUART1_RX TIM2_CH4	LCD_SEG11 EXTI11
31	23	16	16	16	15	VSS	S		Ground	
32	24	17	17	17	16	VDD	S		Digital power supply	
33	25	-	-	-	-	PB12	I/O	FT	EVENTOUT I2C1_SMBA I2C2_SMBA UART3_RTS/UART3_DE UART4_RTS/UART4_DE LPUART1_RTS/LPUART1_DE TIM1_BKIN TIM15_BKIN SPI1_NSS/I2S1_WS SPI2_NSS/I2S2_WS	LCD_SEG12 LCD_VLCD1 EXTI2
34	26	-	-	-	-	PB13	I/O	FT	I2C1_SCL I2C2_SCL UART3_CTS UART4_CTS LPUART1_CTS TIM1_CH1N SPI1_SCK/I2S1_CK SPI2_SCK/I2S2_CK	LCD_SEG13 EXTI3
35	27	-	-	-	-	PB14	I/O	FT	I2C1_SDA I2C2_SDA UART3_RTS/UART3_DE LPUART1_RTS/LPUART1_DE TIM1_CH2N TIM15_CH1 SPI1_MISO/I2S1_MCK SPI2_MISO/I2S2_MCK	LCD_SEG14 EXTI14 OAMP2_IN1+ EXTI14
36	28	-	-	-	-	PB15	I/O	FT	TIM1_CH3N TIM15_CH1N TIM15_CH2 SPI1_MOSI/I2S1_SD SPI2_MOSI/I2S2_SD	LCD_SEG15 RTC_REFIN EXTI15
37	-	-	-	-	-	PC6	I/O	FT	TIM3_CH1	LCD_SEG24 EXTI6
38	-	-	-	-	-	PC7	I/O	FT	TIM3_CH2	LCD_SEG25 EXTI7
39	-	-	-	-	-	PC8	I/O	FT	TIM3_CH3	LCD_SEG26

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

Pin number						Pin Name (Function after reset)	Pin type (1)	5V tolerant	Pin functions	
LQFP64	LQFP48	LQFP32	QFN32	QFN28	TSSOP20				Alternate functions	Additional functions
										EXTI8
40	-	-	-	-	-	PC9	I/O	FT	TIM3_CH4	LCD_SEG27 EXTI9
41	29	18	18	18	-	PA8	I/O	FT	MCO EVENTOUT USART1_CK TIM1_CH1 LPTIM2_IN1 BEEPER CLU0_O CLU1_O CLU2_O CLU3_O	LCD_COM0 EXTI8
42	30	19	19	19	17	PA9	I/O	FT	COMP1_OUT MCO CAN_RX I2C1_SCL USART1_TX USART2_TX UART3_TX LPUART1_TX TIM1_CH2 BEEPER TIM15_BKIN LPTIM2_OUT CLU1_O CLU2_O CLU3_O	LCD_COM1 EXTI9
43	31	20	20	20	18	PA10	I/O	FT	COMP2_OUT CAN_TX I2C1_SDA USART1_RX USART2_RX UART3_RX LPUART1_RX TIM1_CH3 TIM17_BKIN LPTIM2_IN2 BEEPER CLU0_O CLU1_O CLU2_O CLU3_O	LCD_COM2 EXTI10
44	32	21	21			PA11	I/O		COMP1_OUT EVENTOUT USB_DM CAN_RX I2C1_SCL I2C2_SCL USART1_CTS TIM1_CH4 LPTIM2_ETR SPI1_MISO/I2S1_MCK	EXTI11
45	33	22	22			PA12	I/O		COMP2_OUT EVENTOUT USB_DP CAN_TX I2C1_SDA I2C2_SDA	EXTI12

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

Pin number						Pin Name (Function after reset)	Pin type (1)	5V tolerant	Pin functions	
LQFP64	LQFP48	LQFP32	QFN32	QFN28	TSSOP20				Alternate functions	Additional functions
									USART1_RTS/USART1_DE TIM1_ETR SPI1_MOSI/I2S1_SD	
46	34	23	23	21	19	PA13-SWDIO	I/O	FT	SWDIO USB_NOE IROUT	CKI_2 EXTI13
47	35	-	-	-	-	PF6	I/O	FT	USB_NOE BEEPER CLU0_O CLU1_O CLU2_O CLU3_O	EXTI6
48	36	-	-	-	-	VDDIO2	S		Some GPIOs power supply	
49	37	24	24	22	20	PA14-SWCLK	I/O	FT	SWCLK USART1_TX USART2_TX	CKI_3 EXTI14
50	38	25	25	23	-	PA15	I/O	FT	EVENTOUT USART1_RX USART2_RX UART4_RTS/UART4_DE TIM2_CH1/TIM2_ETR SPI1_NSS/I2S1_WS BEEPER	LCD_SEG17 EXTI15
51	-	-	-	-	-	PC10	I/O	FT	UART3_TX UART4_TX LPUART1_TX	LCD_SEG28 LCD_COM4 EXTI10
52	-	-	-	-	-	PC11	I/O	FT	CAN_RX UART3_RX UART4_RX LPUART1_RX	LCD_SEG29 LCD_COM5 EXTI11
53	-	-	-	-	-	PC12	I/O	FT	CAN_TX UART3_CTS UART4_CTS	LCD_SEG30 LCD_COM6 EXTI12
54	-	-	-	-	-	PD2	I/O	FT	UART3_RTS/UART3_DE UART4_RTS/UART4_DE LPUART1_RTS/ LPUART1_DE TIM3_CH1/TIM3_ETR	LCD_SEG31 LCD_COM7 EXTI2
55	39	26	26	24	-	PB3	I/O	FT	EVENTOUT TIM2_CH2 SPI1_SCK/I2S1_CK	COMP2_IN7- LCD_SEG7 EXTI3
56	40	27	27	25	-	PB4	I/O	FT	EVENTOUT UART4_TX TIM3_CH1 TIM17_BKIN SPI1_MISO/I2S1_MCK	COMP2_IN1+ LCD_SEG8 EXTI4
57	41	28	28	26	-	PB5	I/O	FT	I2C1_SMBA UART4_RX TIM3_CH2 TIM16_BKIN LPTIM1_IN1 LPTIM3_IN1 SPI1_MOSI/I2S1_SD	COMP2_IN2+ LCD_SEG9 EXTI5
58	42	29	29	27	-	PB6	I/O	FT	I2C1_SCL USART1_TX LPUART1_TX	COMP2_IN3+ EXTI6

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

Pin number						Pin Name (Function after reset)	Pin type (1)	5V tolerant	Pin functions	
LQFP64	LQFP48	LQFP32	QFN32	QFN28	TSSOP20				Alternate functions	Additional functions
									TIM16_CH1N LPTIM1_ETR LPTIM3_ETR	
59	43	30	30	28	-	PB7	I/O	FT	I2C1_SDA USART1_RX UART4_CTS LPUART1_RX TIM17_CH1N LPTIM1_IN2 LPTIM3_IN2 BEEPER	COMP2_IN4+ PVD_IN EXTI7
60	44	31	31	1	1	Boot0	I	FT	IROUT BEEPER CLU0_O CLU1_O CLU2_O CLU3_O	BOOT0 EXTI8
61	45	-	-	-	-	PB8	I/O	FT	CAN_RX I2C1_SCL TIM16_CH1	LCD_SEG16 EXTI8
62	46	-	-	-	-	PB9	I/O	FT	EVENTOUT CAN_TX I2C1_SDA TIM17_CH1 IROUT SPI2_NSS/I2S2_WS	LCD_COM3 EXTI9
63	47	32	32	-		VSS	S		Ground	
64	48	1	1	-		VDD	S		Digital power supply	

(1). I =input, O=output, I/O= input/output, S=supply.

Note: Unless otherwise specified, all I/Os are set to analog input in the process of reset or after reset.

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

6.8 Alternate Function description

Table 6-2 AF function

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14
PA0/AIN0	-	USART1_CTS	TIM2_CH1/ TIM2_ETR	-	USART2_CTS	-	LPTIM3_IN1	COMP1_OUT	-	UART4_TX	-	-	-	-	-
PA1/AIN1	-	USART1_RTS/ USART1_DE	TIM2_CH2	-	USART2_RTS/ USART2_DE	TIM15_CH1N	LPTIM3_OUT	-	EVENTOUT	UART4_RX	-	-	-	-	-
PA2/AIN2	TIM15_CH1	USART1_TX	TIM2_CH3	-	USART2_TX	-	LPTIM3_IN2	COMP2_OUT	-	-	-	-	-	-	-
PA3/AIN3	TIM15_CH2	USART1_RX	TIM2_CH4	-	USART2_RX	-	LPTIM3_ETR	-	-	-	-	-	-	-	-
PA4/AIN4	SPI1_NSS/ I2S1_WS	USART1_CK	-	-	USART2_CK	UART3_TX	LPTIM2_IN1	-	-	TIM14_CH1	-	-	-	-	-
PA5/AIN5	SPI1_SCK/ I2S1_CK	-	TIM2_CH1/ TIM2_ETR	-		UART3_RX	LPTIM2_OUT	-	-	-		-	-	-	-
PA6/AIN6	SPI1_MISO/ I2S1_MCK	TIM3_CH1	TIM1_BKIN	LPUART1_CTS	CAN_RX	UART3_CTS	LPTIM2_IN2	COMP1_OUT	EVENTOUT	UART4_CTS	TIM16_CH1	-	-	-	-
PA7/AIN7	SPI1_MOSI/ I2S1_SD	TIM3_CH2	TIM1_CH1N	MCO	CAN_TX	UART3_RTS/ UART3_DE	LPTIM2_ETR	COMP2_OUT	EVENTOUT	TIM14_CH1	TIM17_CH1	-	-	-	BEEPER
PA8	MCO	USART1_CK	TIM1_CH1	-	-	-	LPTIM2_IN1	-	EVENTOUT	-	CLU0_O	CLU1_O	CLU2_O	CLU3_O	BEEPER
PA9	TIM15_BKIN	USART1_TX	TIM1_CH2	LPUART1_TX	I2C1_SCL	UART3_TX	LPTIM2_OUT	COMP1_OUT	CAN_RX	USART2_TX	MCO	CLU1_O	CLU2_O	CLU3_O	BEEPER
PA10	TIM17_BKIN	USART1_RX	TIM1_CH3	LPUART1_RX	I2C1_SDA	UART3_RX	LPTIM2_IN2	COMP2_OUT	CAN_TX	USART2_RX	CLU0_O	CLU1_O	CLU2_O	CLU3_O	BEEPER
PA11/ USB_DM	SPI1_MISO/ I2S1_MCK	USART1_CTS	TIM1_CH4	I2C1_SCL	CAN_RX	I2C2_SCL	LPTIM2_ETR	COMP1_OUT	EVENTOUT	-	-	-	-	-	-
PA12/ USB_DP	SPI1_MOSI/ I2S1_SD	USART1_RTS/ USART1_DE	TIM1_ETR	I2C1_SDA	CAN_TX	I2C2_SDA	-	COMP2_OUT	EVENTOUT	-	-	-	-	-	-
PA13_SWDIO	SWDIO	IROUT	USB_NOE	-	-	-	-	-	-	-	-	-	-	-	-
PA14_SWCLK	SWCLK	USART1_TX	-	-	USART2_TX	-	-	-	-	-	-	-	-	-	-
PA15	SPI1_NSS/ I2S1_WS	USART1_RX	TIM2_CH1/ TIM2_ETR	-	USART2_RX	-	-	-	EVENTOUT	UART4_RTS/ UART4_DE	-	-	-	-	BEEPER
PB0/AIN8	-	TIM3_CH3	TIM1_CH2N	-	-	-	-	-	EVENTOUT	-	CLU0_O	CLU1_O	CLU2_O	CLU3_O	BEEPER
PB1/AIN9	TIM14_CH1	TIM3_CH4	TIM1_CH3N	LPUART1_RTS/ LPUART1_DE	-	UART3_RTS/ UART3_DE	LPTIM3_OUT	-	-	UART4_RTS/ UART4_DE	CLU0_O	CLU1_O	CLU2_O	CLU3_O	BEEPER
PB2	-	I2C2_SMBA	-	-	I2C1_SMBA	-	LPTIM1_OUT	-	-	-	-	-	-	-	-
PB3	SPI1_SCK/	-	TIM2_CH2	-	-	-	-	-	EVENTOUT	-	-	-	-	-	-

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14
	I2S1_CK														
PB4	SPI1_MISO/ I2S1_MCK	TIM3_CH1	-	-	-	TIM17_BKIN-	-	-	EVENTOUT	UART4_TX	-	-	-	-	-
PB5	SPI1_MOSI/ I2S1_SD	TIM3_CH2	TIM16_BKIN	I2C1_SMBA	-	-	LPTIM1_IN1	LPTIM3_IN1	-	UART4_RX	-	-	-	-	-
PB6	USART1_TX	I2C1_SCL	TIM16_CH1N	LPUART1_TX	-	-	LPTIM1_ETR	LPTIM3_ETR	-	-	-	-	-	-	-
PB7	USART1_RX	I2C1_SDA	TIM17_CH1N	LPUART1_RX	-	-	LPTIM1_IN2	LPTIM3_IN2	-	UART4_CTS	-	-	-	-	BEEPER
PB8	-	I2C1_SCL	TIM16_CH1	-	CAN_RX	-	-	-	-	-	-	-	-	-	-
PB9	SPI2_NSS/ I2S2_WS	I2C1_SDA	IROUT	TIM17_CH1	CAN_TX	-	-	-	EVENTOUT	-	-	-	-	-	-
PB10	SPI2_SCK/ I2S2_CK	I2C2_SCL	TIM2_CH3	LPUART1_TX	I2C1_SCL		-	UART3_TX	-	UART4_TX	-	-	-	-	-
PB11	-	I2C2_SDA	TIM2_CH4	LPUART1_RX	I2C1_SDA		-	UART3_RX	EVENTOUT	UART4_RX	-	-	-	-	-
PB12	SPI1_NSS/ I2S1_WS	SPI2_NSS/ I2S2_WS	TIM1_BKIN	LPUART1_RTS/ LPUART1_DE	TIM15_BKIN	I2C2_SMBA	I2C1_SMBA	UART3_RTS/ UART3_DE	EVENTOUT	UART4_RTS/ UART4_DE	-	-	-	-	-
PB13	SPI1_SCK/ I2S1_CK	SPI2_SCK/ I2S2_CK	TIM1_CH1N	LPUART1_CTS		I2C2_SCL	I2C1_SCL	UART3_CTS	-	UART4_CTS	-	-	-	-	-
PB14	SPI1_MISO/ I2S1_MCK	SPI2_MISO/ I2S2_MCK	TIM1_CH2N	LPUART1_RTS/ LPUART1_DE	TIM15_CH1	I2C2_SDA	I2C1_SDA	UART3_RTS/ UART3_DE	RTC_OUT		-	-	-	-	-
PB15	SPI1_MOSI/ I2S1_SD	SPI2_MOSI/ I2S2_SD	TIM1_CH3N	TIM15_CH1N	TIM15_CH2	-	-	-	-	-	-	-	-	-	-
PC0/AIN10	-	-	-	-	-	-	LPTIM1_IN1	-	EVENTOUT	-	-	-	-	-	-
PC1/AIN11	-	-	-	-	-	-	LPTIM1_OUT	-	EVENTOUT	-	-	-	-	-	-
PC2/AIN12	-	SPI2_MISO/ I2S2_MCK	-	-	-	-	LPTIM1_IN2	-	EVENTOUT	-	-	-	-	-	-
PC3/AIN13	-	SPI2_MOSI/ I2S2_SD	-	-	-	-	LPTIM1_ETR	-	EVENTOUT	-	-	-	-	-	-
PC4/AIN14	-	-	LPUART1_TX	-	-	UART3_TX	-	-	EVENTOUT	UART4_TX	-	-	-	-	-
PC5/AIN15	-	-	LPUART1_RX	-	-	UART3_RX	-	-	-	UART4_RX	-	-	-	-	-
PC6	TIM3_CH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PC7	TIM3_CH2	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PC8	TIM3_CH3	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PC9	TIM3_CH4	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PC10	-	-	LPUART1_TX	-	-	UART3_TX	-	-	-	UART4_TX	-	-	-	-	-

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14
PC11	-	-	LPUART1_RX		CAN_RX-	UART3_RX	-	-	-	UART4_RX	-	-	-	-	-
PC12	-	-	-	-	CAN_TX-	UART3_CTS	-	-	-	UART4_CTS	-	-	-	-	-
PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PC14_X0A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PC15_X1A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PD2	TIM3_CH1/ TIM3_ETR	-	LPUART1_RTS/ LPUART1_DE	-	-	UART3_RTS/ UART3_DE	-	-	-	UART4_RTS/ UART4_DE	-	-	-	-	-
PF0_OSC_ IN	-	I2C1_SDA	-	-	-	-	-	-	-	-	-	-	-	-	-
PF1_OSC_OUT	-	I2C1_SCL	-	-	-	-	-	-	-	-	-	-	-	-	-
PF4	-	-	-	-	-	-	-	-	EVENTOUT	-	CLU0_O	CLU1_O	CLU2_O	CLU3_O	BEEPER
PF5	-	-	-	-	-	-	-	-	EVENTOUT	-	CLU0_O	CLU1_O	CLU2_O	CLU3_O	BEEPER
PF6	-	-	USB_NOE	-	-	-	-	-	-	-	CLU0_O	CLU1_O	CLU2_O	CLU3_O	BEEPER
BOOT0_PF8	-	-	IROUT	-	-	-	-	-	-	-	CLU0_O	CLU1_O	CLU2_O	CLU3_O	BEEPER

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

7 Package characteristics

7.1 LQFP64

LQFP64 is a 10 x 10 mm and 0.5 mm pitch package.

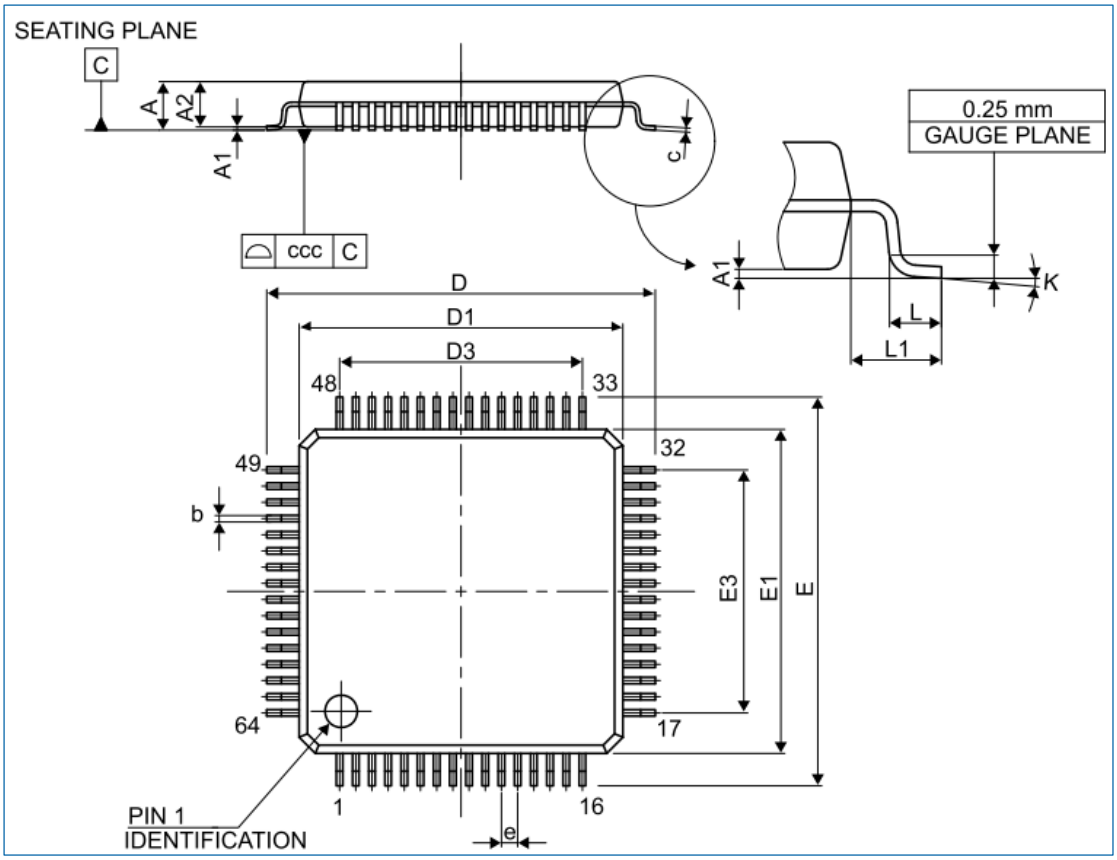


Figure 7-1 LQFP64 package outline

Table 7-1 LQFP64 package parameters

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.5000	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

(1). Values in inches are converted from mm and rounded to 4 decimal digits.

7.2 LQFP48

LQFP48 is a 7 mm x 7 mm and 0.5 mm pitch package.

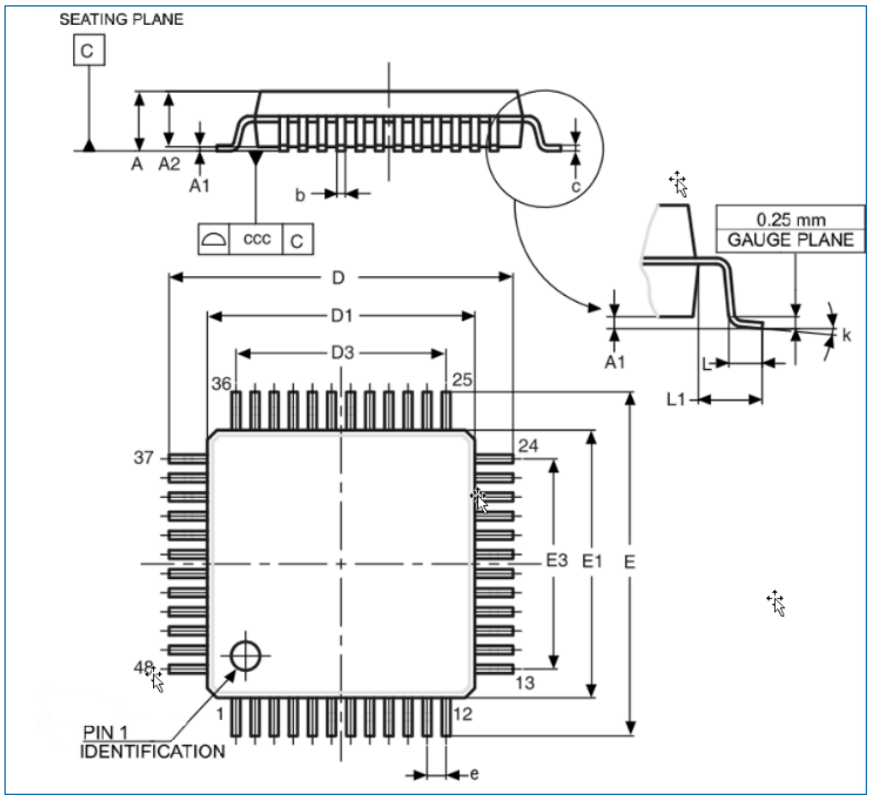


Figure 7-2 LQFP48 package outline

Table 7-2 LQFP48 package parameters

Symbol	millimeters			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
B	0.170	0.220	0.270	0.0067	0.0087	0.0106
C	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
E	-	0.500	-	-	0.0197	-

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

Symbol	millimeters			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
K	0°	3.5°	7°	0°	3.5°	7°
Ccc	0.080			0.0031		

(1). Values in inches are converted from mm and rounded to 4 decimal digits.

7.3 LQFP32

LQFP32 is a 7 mm x 7 mm and 0.8 mm pitch package.

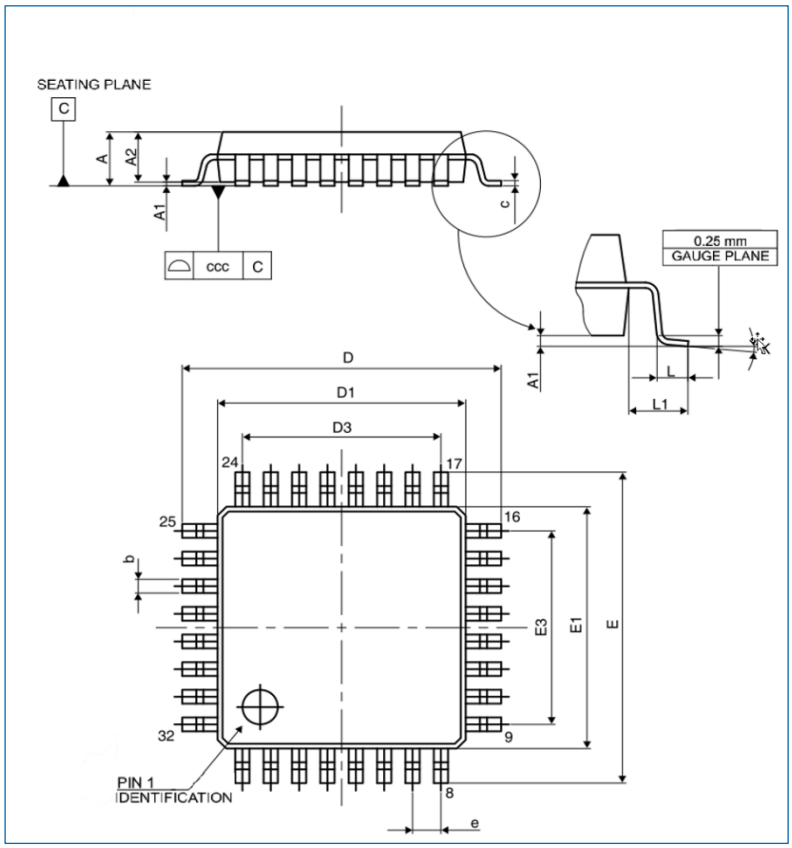


Figure 7-3 LQFP32 package outline

Table 7-3 LQFP32 package parameters

Symbol	millimeters			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
B	0.300	0.370	0.450	0.0118	0.0146	0.0177
C	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

Symbol	millimeters			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
E	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
K	0°	3.5°	7°	0°	3.5°	7°
Ccc	0.100			0.0039		

(1). Values in inches are converted from mm and rounded to 4 decimal digits.

7.4 QFN32

QFN32 is a 5 mm x 5 mm and 0.5 mm pitch package.

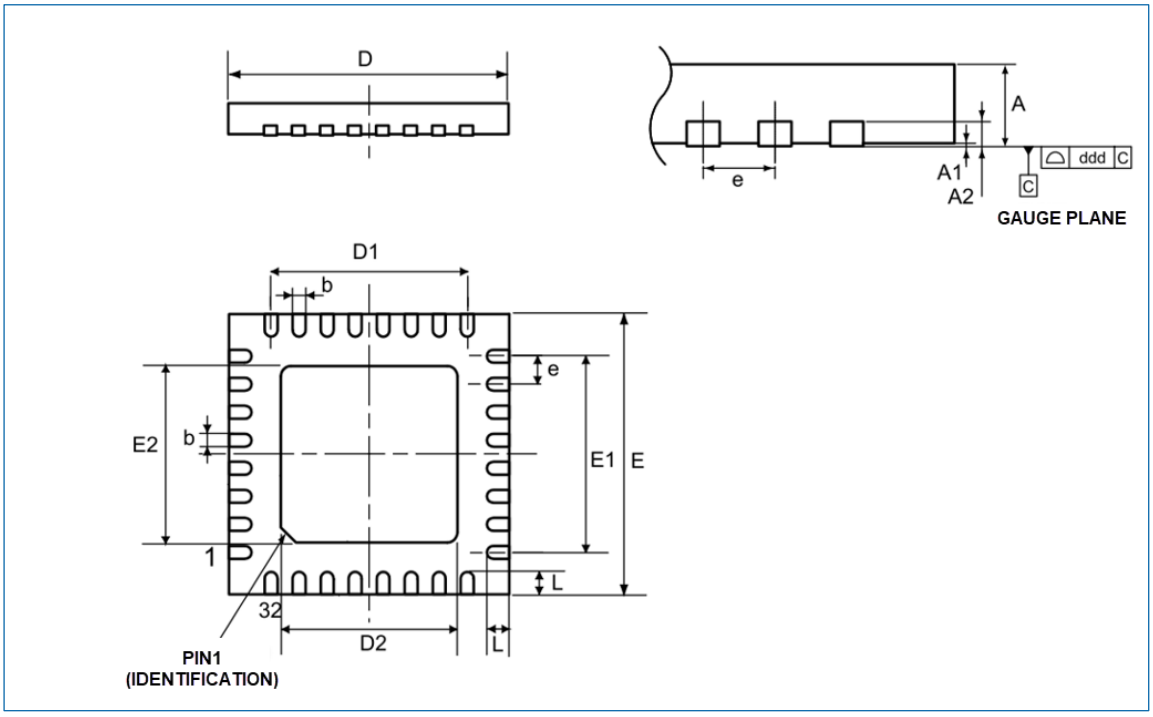


Figure 7-4 QFN32 package outline

Table 7-4 QFN32 package parameters

Symbol	Unit: mm			Unit: inches [1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.500	0.550	0.600	0.0197	0.0217	0.0236
A2	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	0.230	0.280	0.0071	0.0091	0.0110
D	4.900	5.000	5.100	0.1929	0.1969	0.2008
D1	3.400	3.500	3.600	0.1339	0.1378	0.1417
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
E	4.900	5.000	5.100	0.1929	0.1969	0.2008

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

Symbol	Unit: mm			Unit: inches (1)		
	Min	Typ	Max	Min	Typ	Max
E1	3.400	3.500	3.600	0.1339	0.1378	0.1417
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

(1). Values in inches are converted from mm and rounded to 4 decimal digits.

7.5 QFN28

QFN28 is a 4 mm x 4 mm, 0.4 mm pitch package。

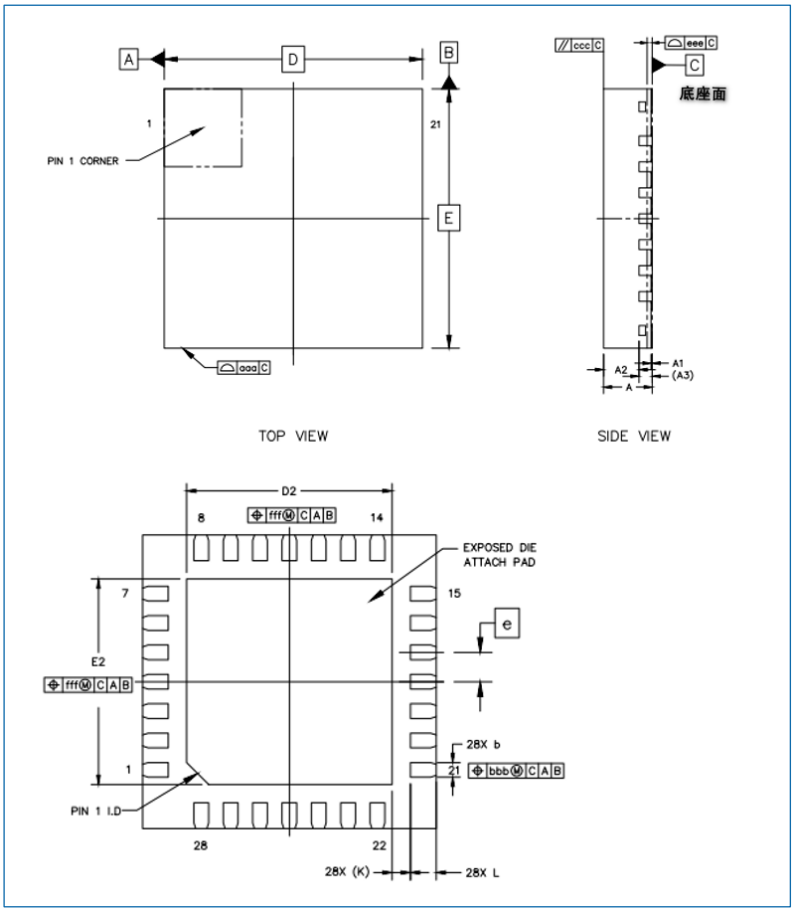


Figure 7-5 QFN28 package outline

Table 7-5 QFN28 package parameters

Symbol	Min (mm)	Typ (mm)	Max (mm)
A	0.7	0.75	0.8
A1	0	0.02	0.05
A2	-	0.55	-
A3	0.203REF (1)		
b	0.15	0.20	0.25
D	4BSC (2)		
E	4BSC		

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

Symbol	Min (mm)	Typ (mm)	Max (mm)
e	0.4BSC		
D2	2.7	2.9	2.9
E2	2.7	2.9	2.9
L	0.3	0.35	0.4
K	0.25REF		
aaa	0.1		
ccc	0.1		
eee	0.08		
bbb	0.1		
fff	0.1		

(1). REF: Reference，表示参考值。

(2). BSC: Basic spacing between centers，即中心基本距离。

7.6 TSSOP20

TSSOP20 is a 6.5 mm x 6.5 mm, 0.65 mm pitch package.

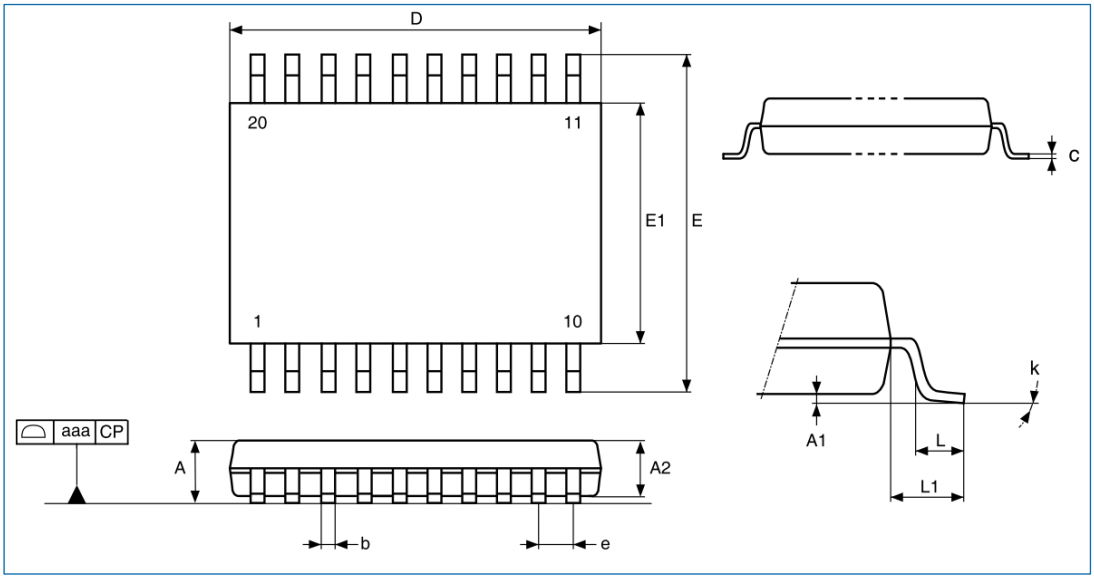


Figure 7-6 TSSOP20 package outline

Table 7-6 TSSOP20 package parameters

Symbol	Unit: mm			Unit: inches (1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D	6.400	6.500	6.600	0.2520	0.2559	0.2598
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1	4.300	4.400	4.500	0.1693	0.1732	0.1772

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

Symbol	Unit: mm			Unit: inches (1)		
	Min	Typ	Max	Min	Typ	Max
e	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	-	8.0°	0°	-	8.0°
aaa	-	-	0.1000	-	-	0.0039

(1). Values in inches are converted from mm and rounded to 4 decimal digits.

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

8 Ordering information

Table 8-1 ordering information

Package type	Model	Packaging	Comments
LQFP64	HK32L084RBT6/ HK32L0H4RBT6	Tape and reel/Tray	-
	HK32L088RBT6/ HK32L0H8RBT6	Tape and reel/Tray	-
LQFP48	HK32L084CBT6/ HK32L0H4CBT6	Tape and reel/Tray	-
	HK32L088CBT6/ HK32L0H8CBT6	Tape and reel/Tray	-
LQFP32	HK32L084KBT6/ HK32L0H4KBT6	Tape and reel/Tray	
	HK32L088KBT6/ HK32L0H8KBT6	Tape and reel/Tray	
QFN32	HK32L084KBU6/ HK32L0H4KBU6	Tape and reel/Tray	
	HK32L088KBU6/ HK32L0H8KBU6	Tape and reel/Tray	
QFN28	HK32L084GBU6/ HK32L0H4GBU6	Tape and reel/Tray	
	HK32L088GBU6/ HK32L0H8GBU6	Tape and reel/Tray	
TSSOP20	HK32L084FBP6/ HK32L0H4FBP6	Tape and reel/Tube	
	HK32L088FBP6/ HK32L0H8FBP6	Tape and reel/Tube	

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

9 Glossary and Abbreviations

Name	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
AWU	Auto-Wakeup
CRC	Cyclic Redundancy Check
CSS	Clock Security System
DMA	Direct Memory Access
EEPROM	Electrically Erasable Programmable Read Only Memory
EXTI	Extended Interrupts and Events Controller
GPIO	General Purpose Input Output
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IWDG	Independent Watchdog
LSI	Low-Speed Internal (Clock Signal)
MCU	Microcontroller Unit
MSPS	Million Samples Per Second
NVIC	Nested Vectored Interrupt Controller
PDR	Power-Down Reset
PLL	Phase Locked Loop
POR	Power-On Reset
PWM	Pulse Width Modulation
RCC	Reset and Clock Control
RISC	Reduced Instruction Set Computing
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SWD	Serial Wire Debug
USART	Universal Synchronous Asynchronous Receiver Transmitter
WWDG	Window Watchdog

Copyright © 2023 Shenzhen Hangshun Chip Technology R&D Co., Ltd

10 Legal and Contact Information

航顺芯片 and other Hangshun trademarks are trademarks of Shenzhen Hangshun Chip Technology R&D Co., Ltd. All other trademarks or trade names mentioned in this document are the property of their respective holders.

Without the consent of Shenzhen Hangshun Chip Technology R&D Co., Ltd., any part and sub-part of the company's product specifications and datasheets must not be modified in any form or way. Shenzhen Hangshun Chip Technology R&D Co., Ltd. reserves the right to modify the data sheet and/or products, discontinue any product or terminate the service without notice. It is recommended that customers obtain the latest version of relevant information and verify before placing an order. Ensure the timelines and completeness of the information. All products are sold in accordance with the terms of the sales contract provided at the time of order confirmation. The terms include the scope of warranty, intellectual property rights and the scope of responsibility.

Shenzhen Hangshun Chip Technology R&D Co., Ltd. guarantees that the performance of the product is guaranteed in accordance with the company's standard during the sales period. The company believes it is necessary to maintain this warranty and will use testing and other quality control techniques. Except for mandatory government regulations, there is no need for special tests for measuring by other instruments.

The customer acknowledges that the purpose of the design and production of the company's products does not involve life support or used in other dangerous activities or other systems or products in the environment. Malfunctioning products can cause personal injury or death, property, or environmental damage (collectively referred to as high-risk activities). The company's products are artificially used in high-risk activities, and the company does not guarantee it and is not liable to customers or third parties.

Shenzhen Hangshun Chip Technology R&D Co., Ltd. will provide the same technical support, help, advice, and information as it is now (including the design, development or debugging of the purchased circuit board or other applications). Hereby declare that for all technical support, marketability or for a specific purpose, and if the circuit board and other applications can be operated or run under the correct technical support, the company will not make any guarantee for such support technology, and no legal responsibility for your use of this support service.

Copyright © Shenzhen Hangshun Chip Technology R&D Co., Ltd 2015-2022

Shenzhen Hangshun Chip Technology R&D Co., Ltd

TEL: +86-755-83247667

Website: www.hsxp-hk.com