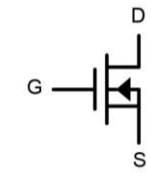
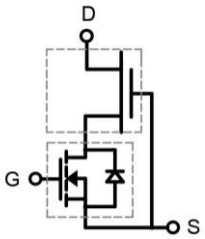
## Features

- Easy to use, compatible with standard gate drivers
- Excellent $Q_G$ x $R_{DS(on)}$ figure of merit (FOM)
- Low $Q_{RR}$, no free-wheeling diode required
- Low switching loss
- RoHS compliant and Halogen-free
- Qualified according to JEDEC criteria

| Product Summary | | |
|---|---|---|
| $V_{DSS}$ | 700 | V |
| $R_{DS(on),typ}$ | 125 | mΩ |
| $Q_{G,typ}$ | 16 | nC |
| $Q_{RR,typ}$ | 36 | nC |



Schematic Symbol



Cascode
Device Structure



## Applications

- High efficiency power supplies
- Telecom and datacom
- Automotive
- Servo motors

### Packaging

| Part Number | Marking | Package | Packaging | Base QTY |
|---|---|---|---|---|
| CRND125C70H | CRND125C70H | TO-252 | Tape and Reel | 2500 |

### Maximum ratings, at $T_C$=25 ° C, unless otherwise specified

| Symbol | Parameter | | Limit Value | Unit |
|---|---|---|---|---|
| $I_D$ | Continuous drain current @$T_C$=25 ° C | | 18.4 | A |
| | Continuous drain current @$T_C$=100 ° C | | 11.7 | A |
| $I_{DM}$ | Pulsed drain current @$T_C$=25 ° C (pulse width: 100us) | | 49 | A |
| | Pulsed drain current @$T_C$=150 ° C (pulse width: 100us) | | 37 | A |
| $V_{DSS}$ | Drain to source voltage ($T_J$ = -55 ° C to 150 ° C) | | 700 | V |
| $V_{TDSS}$ | Transient drain to source voltage [a] | | 800 | V |
| $V_{GSS}$ | Gate to source voltage | | ±20 | V |
| $P_D$ | Maximum power dissipation @$T_C$=25 ° C | | 89 | W |
| $T_C$ | Operating temperature | Case | -55 to 150 | ° C |
| $T_J$ | | Junction | -55 to 150 | ° C |
| $T_S$ | Storage temperature | | -55 to 150 | ° C |
| $T_{CSOLD}$ | Soldering peak temperature | | 260 | ° C |

## Thermal Resistance

| Symbol | Parameter | Typical | Unit |
|---|---|---|---|
| $R_{\Theta JC}$ | Junction-to-case | 1.4 | °C/W |
| $R_{\Theta JA}$ | Junction-to-ambient [b] | 50 | °C/W |

Notes:
a. Off-state spike duty cycle < 0.01, spike duration < 2us
b. Device on one layer epoxy PCB for drain connection (vertical and without air stream cooling, with 6cm$^2$copper area and 70μm thickness)

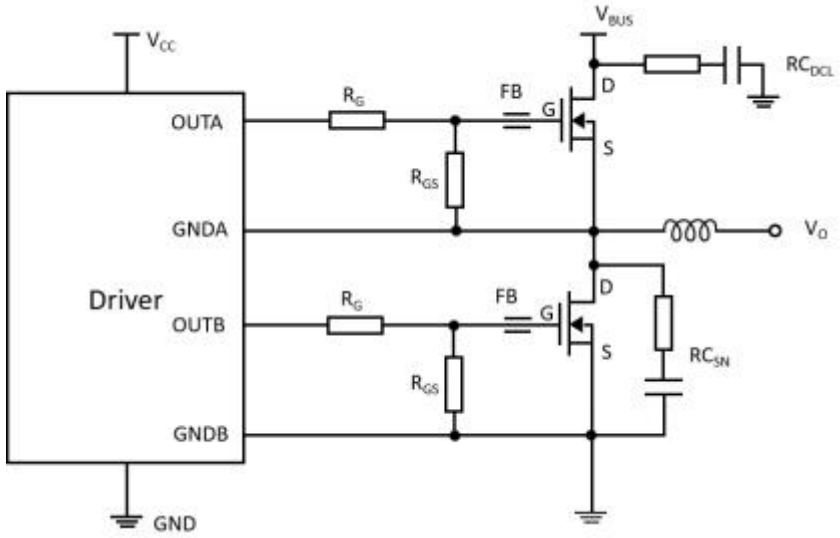
## Electrical Parameters, at $T_J$=25 ° C, unless otherwise specified

| Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| **Forward Characteristics** | | | | | |
| $V_{DSS-MAX}$ | 700 | - | - | V | $V_{GS}$=0V |
| $BV_{DSS}$ | - | 1000 | - | | $V_{GS}$=0V, $I_{DSS}$=250 μA |
| $V_{GS(th)}$ | 3 | 4 | 5 | V | $V_{DS}$=$V_{GS}$, $I_D$=500 μA |
| $\triangle V_{GS(th)}/T_J$ | - | -10.3 | - | mV/℃ | |
| $R_{DS(on)}$ [c] | - | 125 | 160 | mΩ | $V_{GS}$=12V, $I_D$=4A, $T_J$=25° C |
| | - | 250 | - | | $V_{GS}$=12V, $I_D$=4A, $T_J$=150° C |
| $I_{DSS}$ | - | 6 | 20 | μA | $V_{DS}$=700V, $V_{GS}$=0V, $T_J$=25° C |
| | - | 50 | - | μA | $V_{DS}$=700V, $V_{GS}$=0V, $T_J$=150° C |
| $I_{GSS}$ | - | - | 150 | nA | $V_{GS}$=20V |
| | - | - | -150 | nA | $V_{GS}$=-20V |
| $C_{ISS}$ | - | 538 | - | pF | $V_{GS}$=0V, $V_{DS}$=400V, f=1MHz |
| $C_{OSS}$ | - | 28 | - | pF | |
| $C_{RSS}$ | - | 1 | - | pF | |
| $C_{O(er)}$ | - | 42 | - | pF | $V_{GS}$=0V, $V_{DS}$=0 - 400V |
| $C_{O(tr)}$ | - | 91 | - | pF | |
| $Q_{OSS}$ | - | 36 | - | nC | |
| $Q_G$ | - | 16 | - | nC | $V_{DS}$=400V, $V_{GS}$=0 - 12V, $I_D$=11.7A |
| $Q_{GS}$ | - | 3.6 | - | | |
| $Q_{GD}$ | - | 4.7 | - | | |
| $t_{D(on)}$ | - | 20 | - | ns | $V_{DS}$=400V, $V_{GS}$=0 - 12V, $I_D$=11.7A, $R_G$=47Ω |
| $t_R$ | - | 16 | - | | |
| $t_{D(off)}$ | - | 46 | - | | |
| $t_F$ | - | 6 | - | | |
| **Reverse Characteristics** | | | | | |
| $V_{SD}$ | - | 1.5 | - | V | $V_{GS}$=0V, $I_S$=6A, $T_J$=25° C |
| | - | 2.2 | - | | $V_{GS}$=0V, $I_S$=12A, $T_J$=25° C |
| | - | 3.1 | - | | $V_{GS}$=0V, $I_S$=12A, $T_J$=150° C |
| $t_{RR}$ | - | 21 | - | ns | $I_S$=11.7A, $V_{GS}$=0V, $d_i/d_t$=1000A/us, $V_{DD}$=400V |
| $Q_{RR}$ | - | 36 | - | nC | |

Notes:
c. Dynamic on-resistance; see Figure 20 and 21 for test circuit and configurations

## Circuit Implementation

Mostly used in half bridge and full bridge topology




**Recommended Half-bridge Circuit**

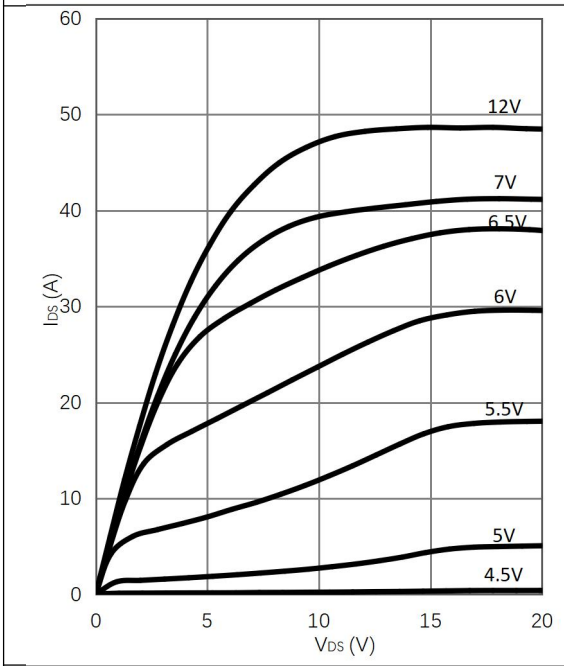
Recommended gate drive: (0 V, 12 V)

| Gate Ferrite Bead (FB) | Gate Resistance ($R_G$) | Gate Source Resistance ($R_{GS}$) | Switching RC Snubber ($RC_{SN}$) | DC Link RC Snubber ($RC_{DCL}$) |
|---|---|---|---|---|
| 300 - 600 Ω @100MHz | 33 Ω | 10 kΩ | 15 Ω + 47 nF | 5 Ω + 4.7 nF |

Notes:
d. $RC_{SN}$ should be placed as close as possible to the drain pin
e. The layout and wiring of the drive circuit should be as short as possible

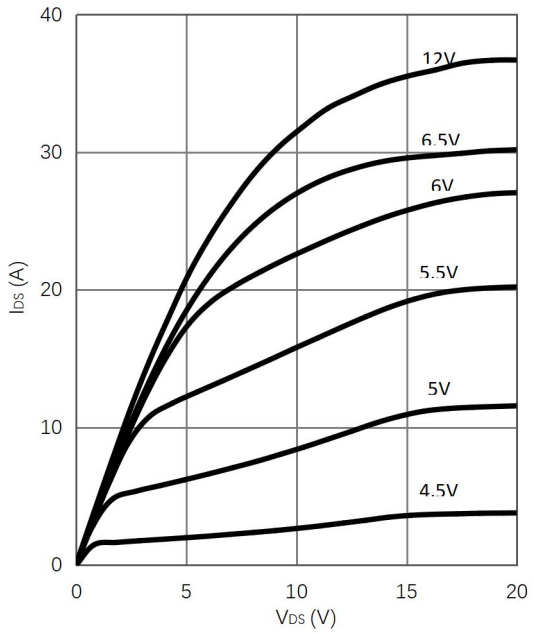
## Typical Characteristics, at $T_C$=25 ° C, unless otherwise specified

**Figure 1. Typical Output Characteristics $T_J$=25° C**



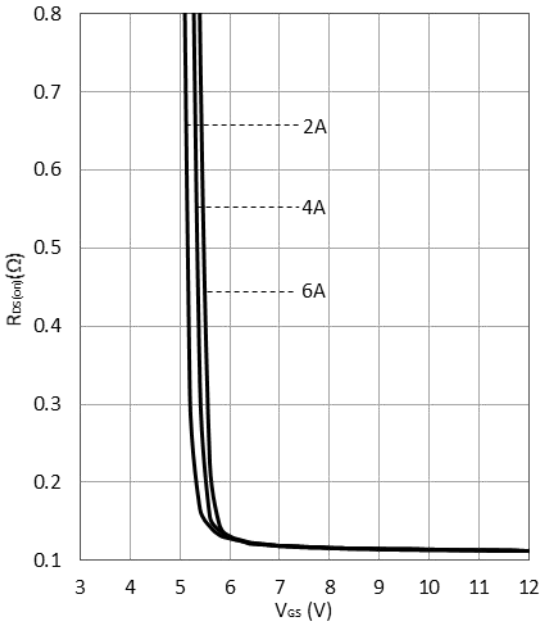

Parameter: $V_{GS}$

**Figure 2. Typical Output Characteristics $T_J$=150° C**



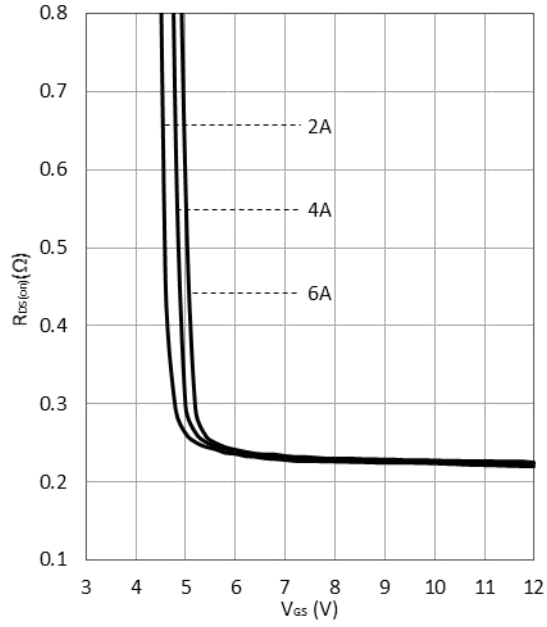

Parameter: $V_{GS}$

**Figure 3.Typical Drain to Source On-resistance TJ= 25° C**



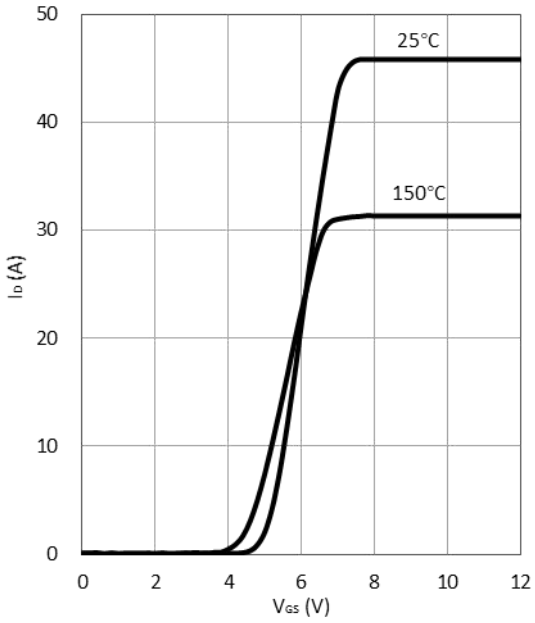

Parameter: $I_D$

**Figure 4. Typical Drain to Source On-resistance $T_J$= 150° C**



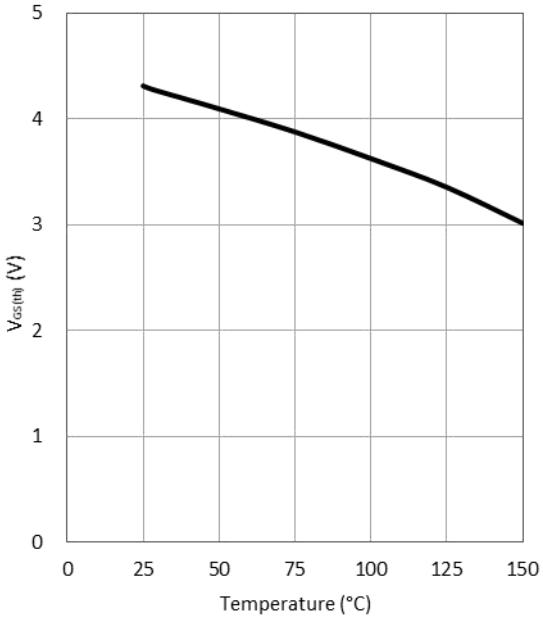

Parameter: $I_D$

**Figure 5. Typical Transfer Characteristics**



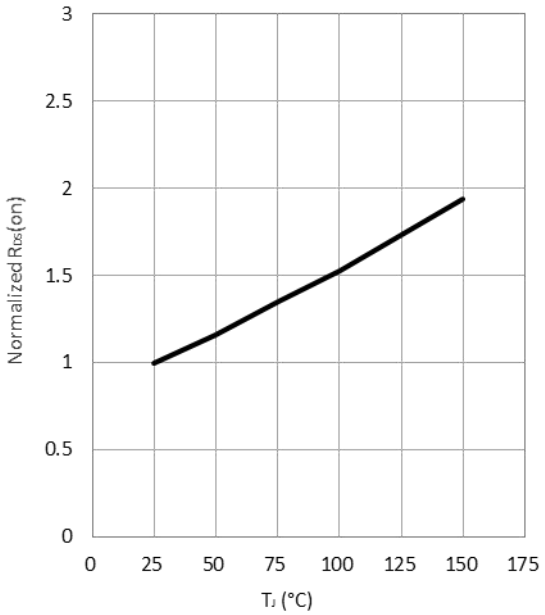

$V_{DS}$=10V, Parameter: $T_J$

**Figure 6. $V_{GS(th)}$ Vs Temperature Characteristics**



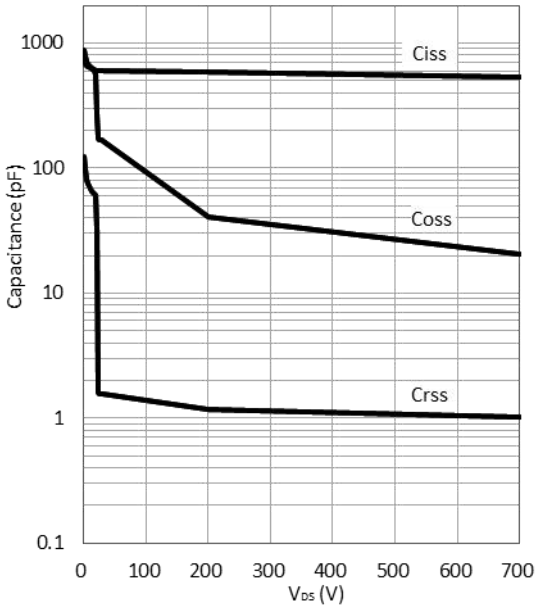

$I_D$=500uA

**Figure 7. Normalized On-resistance**



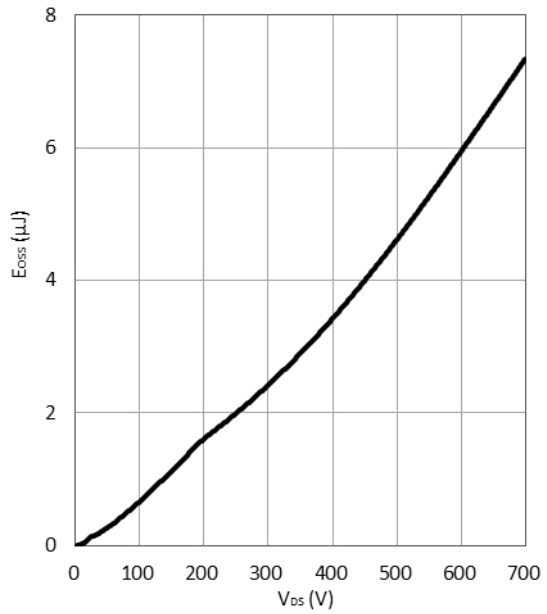

$I_D$=4A, $V_{GS}$=12V

**Figure 8. Typical Capacitance**



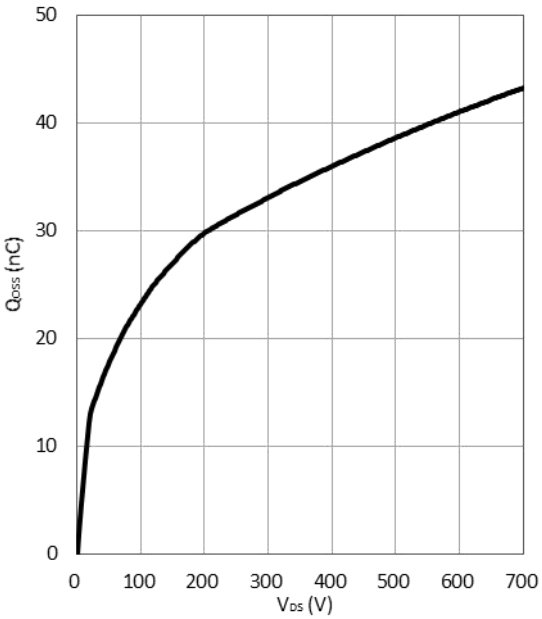

$V_{GS}$=0V, f=1MHz

**Figure 9. Typical Coss Stored Energy**



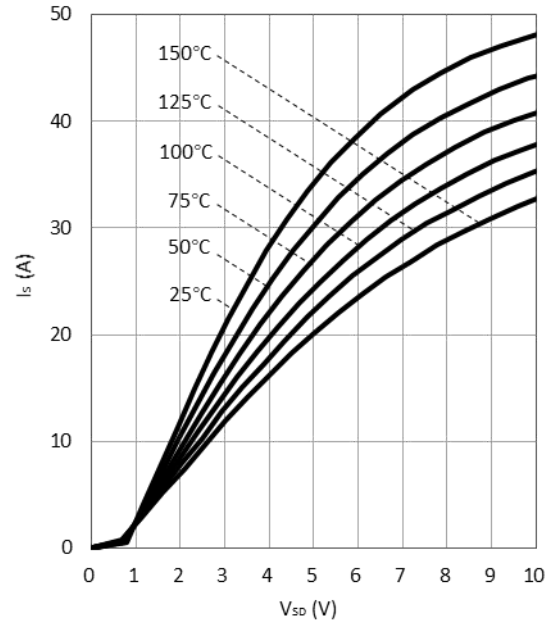

$V_{GS}$=0V, f=1MHz

**Figure 10. Typical Qoss**



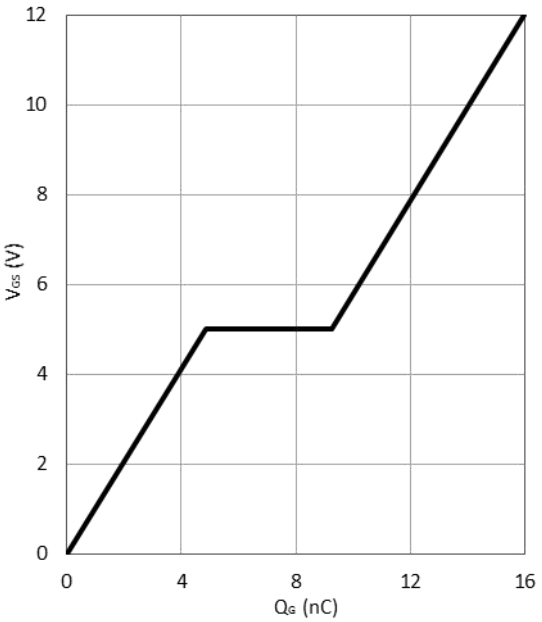

$V_{GS}$=0V, f=1MHz

**Figure 11. Forward Characteristic of Rev. Diode**




$I_S=f(V_{SD})$, Parameter $T_J$

**Figure 12. Typical Gate Charge**




$I_{DS}$=12A, $V_{DS}$=400V

**Figure 13. Power Dissipation**

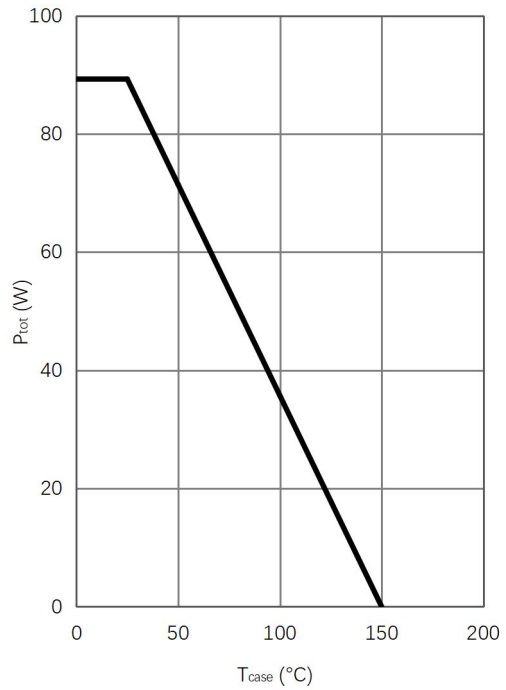



**Figure 14. Current Derating**

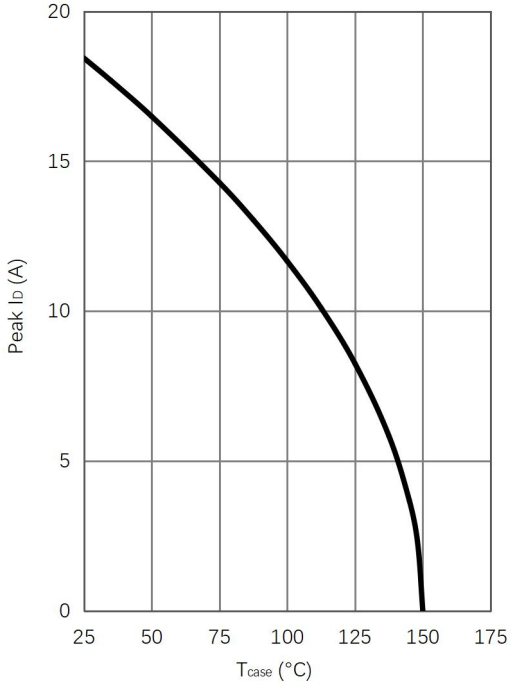



**Figure 15. Transient Thermal Resistance**

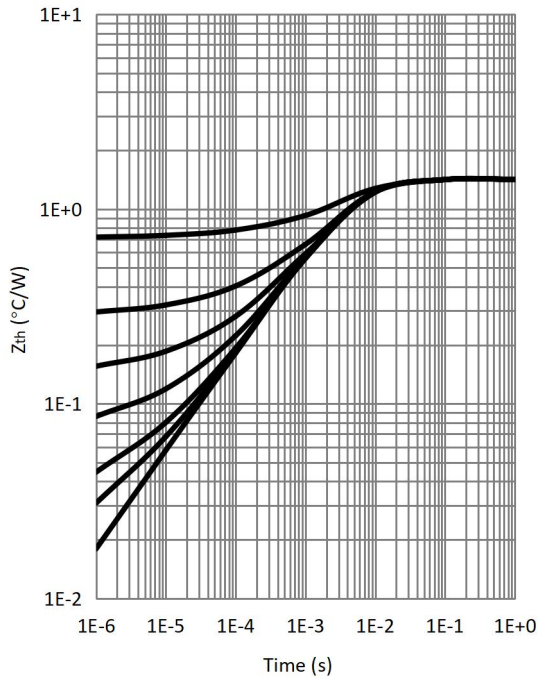
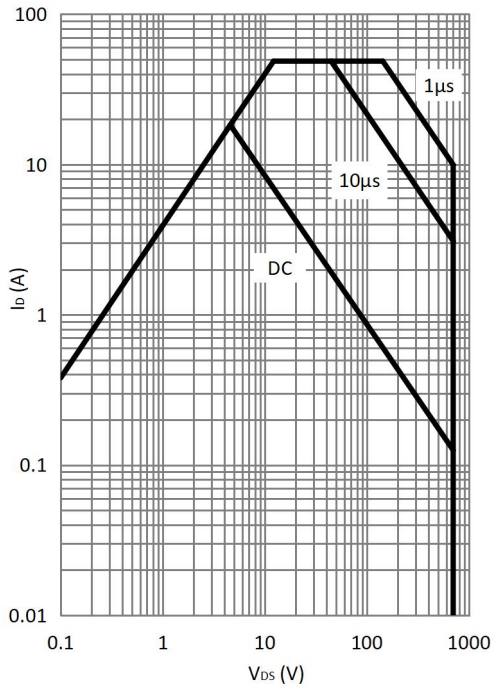
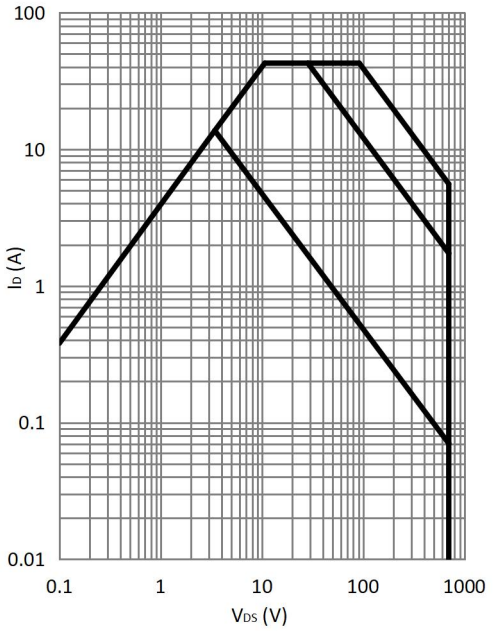



**Figure 16. Safe Operating Area $T_C$=25° C**



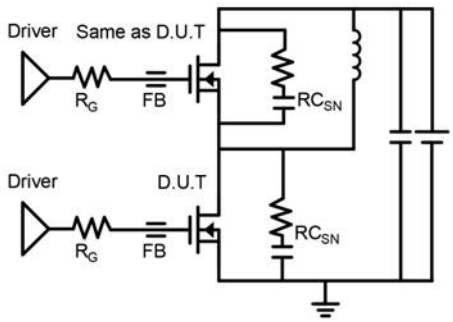
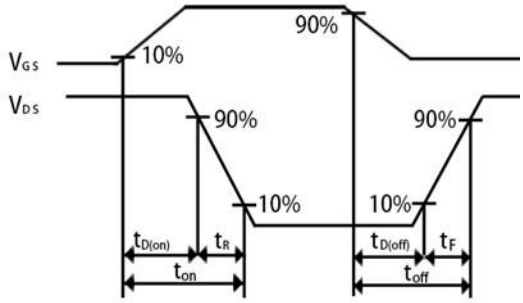

calculated based on thermal limit

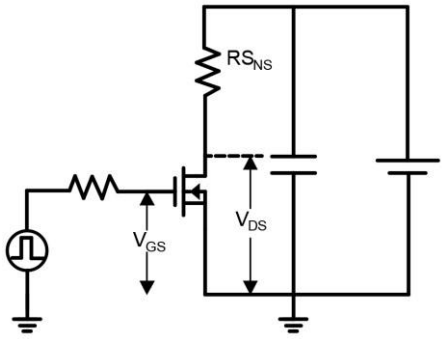
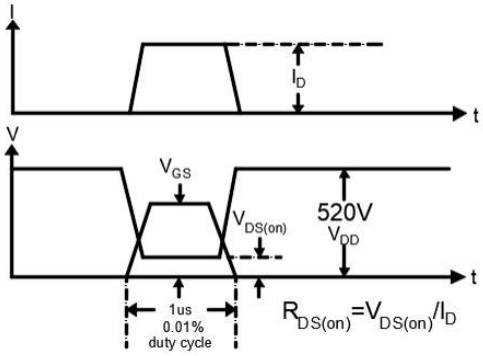
**Figure 17. Safe Operating Area $T_C$=80° C**

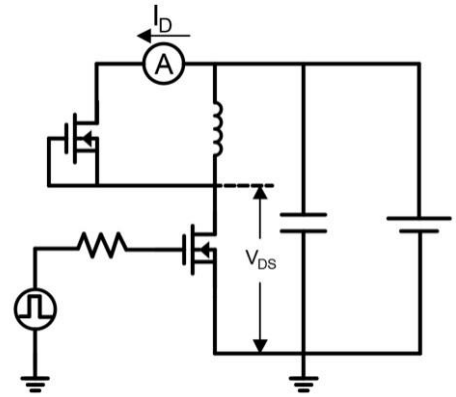
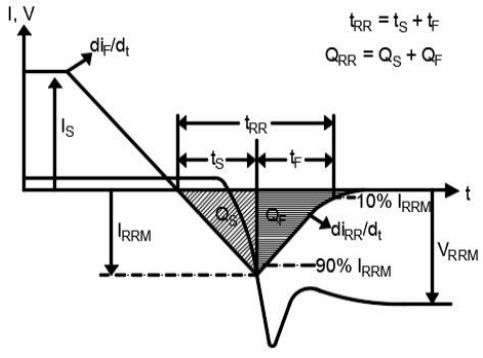



calculated based on thermal limit

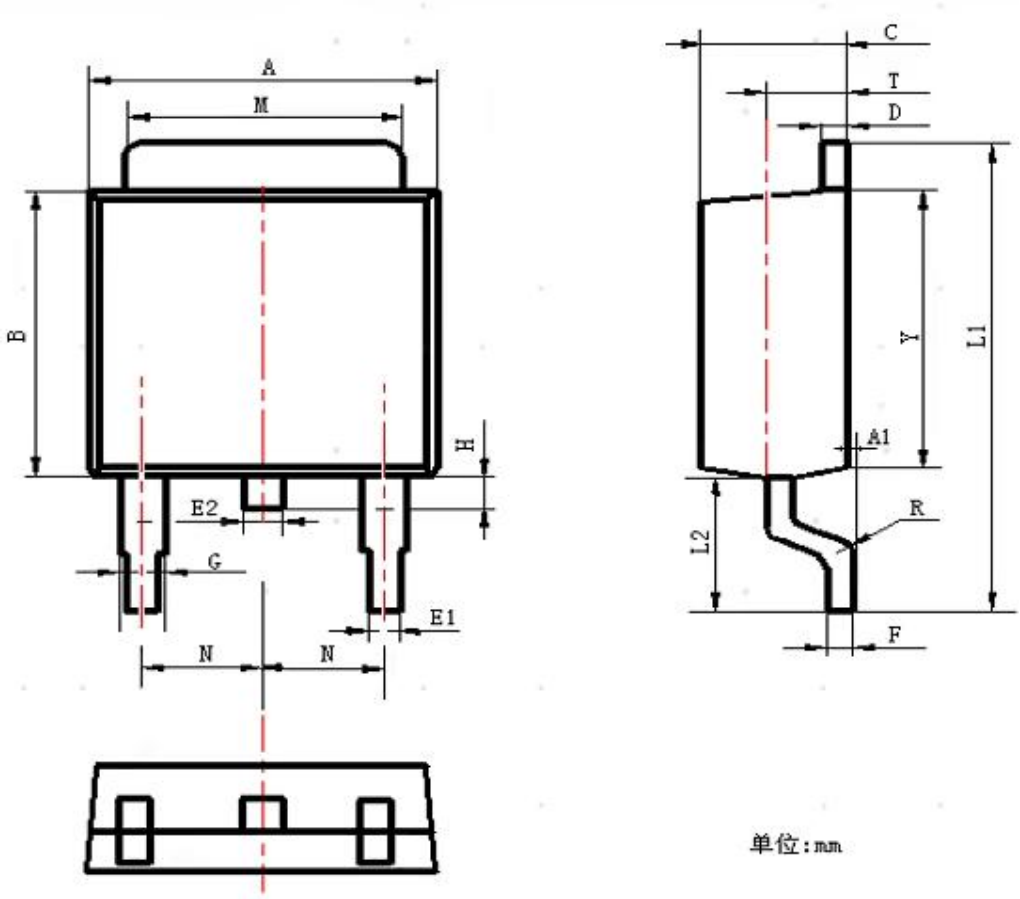
## Test Circuits and Waveforms

| Figure 18. Switching Time Test Circuit | Figure 19. Switching Time Waveform |
|---|---|
|  |  |

| Figure 20. Dynamic $R_{DS(on)}$ Test Circuit | Figure 21. Dynamic $R_{DS(on)}$ Waveform |
|---|---|
|  |  |

| Figure 22. Diode Characteristic Test Circuits | Figure 23. Diode Recovery Waveform |
|---|---|
|  |  |

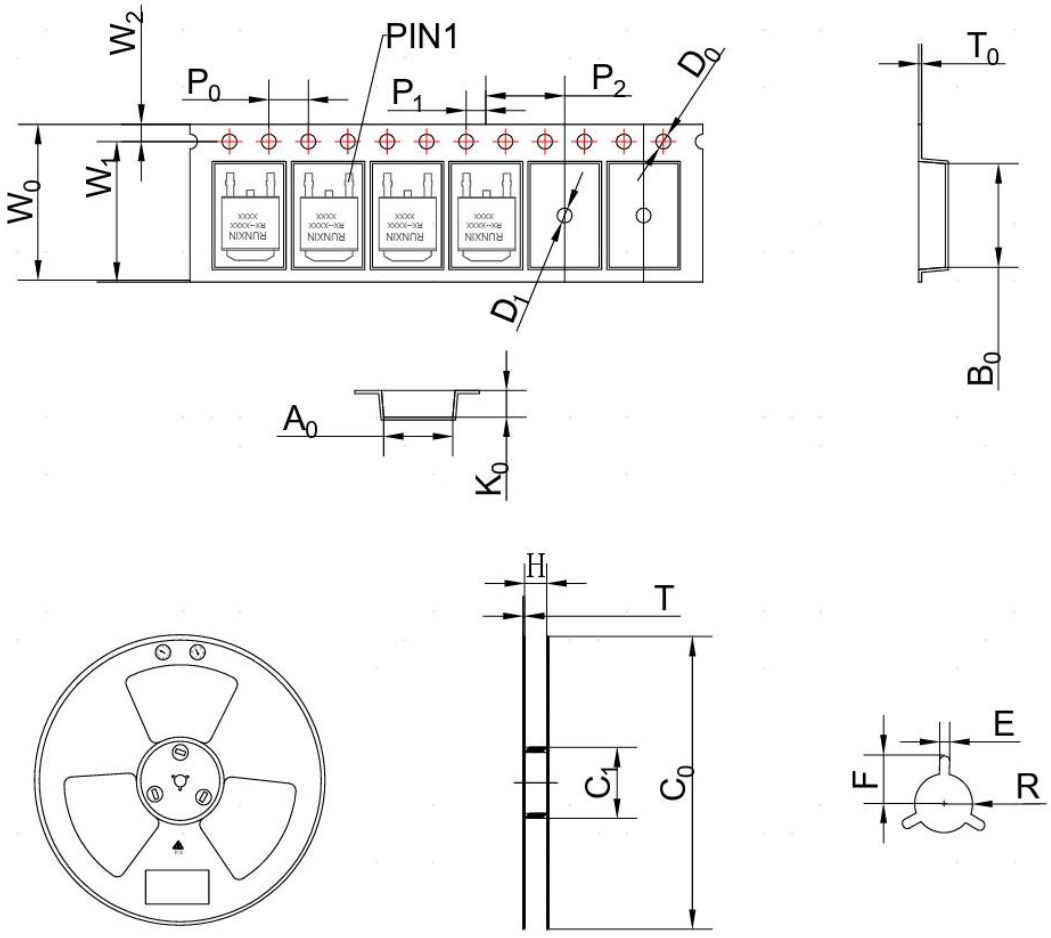
## Package Outline




| SYMBOL | Millimeter | | |
|---|---|---|---|
| | Min | Nom | Max |
| A | 6.30 | 6.60 | 6.90 |
| A1 | 0 | 0.80 | 0.16 |
| B | 5.70 | 6.00 | 6.30 |
| C | 2.10 | 2.30 | 2.50 |
| D | 0.30 | 0.60 | 0.90 |
| E1 | 0.60 | 0.75 | 0.90 |
| F | 0.30 | 0.45 | 0.60 |
| G | 0.70 | 0.95 | 1.20 |
| L1 | 9.30 | 9.90 | 10.50 |
| L2 | 2.50 | 2.80 | 3.10 |
| H | 0.40 | 0.70 | 1.05 |
| M | 4.90 | 5.30 | 5.60 |
| N | 2.09 | 2.29 | 2.49 |

## Tape and Reel Information

Dimensions are shown in millimeters





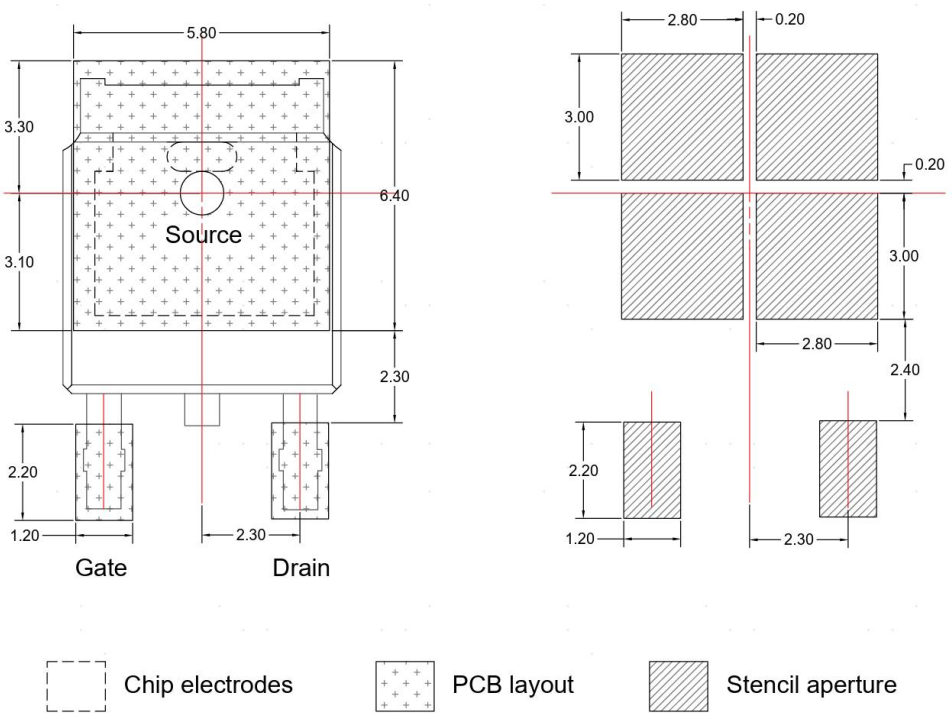


| Tape Dimension | | | | | |
|---|---|---|---|---|---|
| $W_0$ | 16+0.3-0.2 | $P_0$ | 4±0.1 | $A_0$ | 7±0.1 |
| $W_1$ | 14.25±0.1 | $P_1$ | 2±0.1 | $B_0$ | 10.5±0.1 |
| $W_2$ | 1.75±0.1 | $P_2$ | 8±0.1 | $D_1$ | 1.5±0.25 |
| $K_0$ | 2.7±0.1 | $D_0$ | 1.5±0.1 | $T_0$ | 0.3±0.05 |

| Reel Dimension | | | |
|---|---|---|---|
| H | 17±0.1 | F | 10.5±0.1 |
| T | 2±0.2 | E | 2.8±0.1 |
| $C_0$ | 330±3 | R | 6.5±0.1 |
| $C_1$ | 100±1 | | |

**Recommended PCB Layout & Stencil apertures**

**Dimensions are shown in millimeters**



## Revision History

| Version | Date | Change(s) |
|---|---|---|
| 1.0 | 2025/12/01 | Release Formal Datesheet |

## Disclaimer

Unless otherwise specified in the datasheet, the product is designed and qualified as a standard commercial product and is not intended for use in applications that require extraordinary levels of quality and reliability, such as automotive, aviation/aerospace and life-support devices or systems.

Any and all semiconductor products have certain probability to fail or malfunction, which may result in personal injury, death or property damage. Customer are solely responsible for providing adequate safe measures when design their systems.