CRSY030N04L2Q

SkyMOS2 N-MOSFET 40V, 1.7mΩ, 140A

Features

- Uses CRM(CQ) advanced SkyMOS2 technology
- Extremely low on-resistance $R_{DS(on)}$
- Excellent Q_gx$R_{DS(on)}$ product(FOM)
- AEC-Q101 Qualified

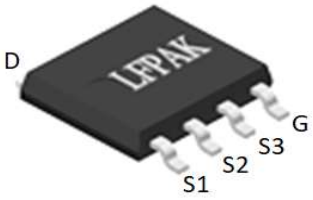
Product Summary

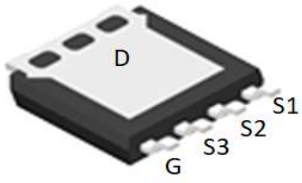
V_{DS}	40V
$R_{DS(on).typ}$	1.7mΩ
I_D	140A

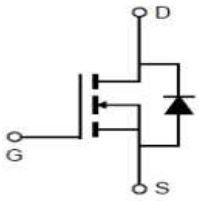
100% DVDS Tested
100% Avalanche Tested

Applications

- Motor control and drive
- Battery management System







CRSY030N04L2Q

Package Marking and Ordering Information

Part #	Marking	Package	Packing	Reel Size	Tape Width	Qty
CRSY030N04L2Q	030N04L2Q	LFPAK5*6	Tape&reel	N/A	N/A	4000pcs

Absolute Maximum Ratings

Parameter	**Symbol**	**Value**	**Unit**
Drain-source voltage	V_{DS}	40	V
Continuous drain current T_C = 25°C (Silicon limit) T_C = 100°C (Silicon limit)	I_D	 140 96	A
Pulsed drain current (T_C = 25°C, t_p limited by T_{jmax})	$I_{D\ pulse}$	560	A
Avalanche energy, single pulse (I_D = 32A, Rg=25Ω)[1]	E_{AS}	153	mJ
Gate-Source voltage	V_{GS}	±20	V
Power dissipation (T_C = 25°C)	P_{tot}	124	W
Operating junction and storage temperature	T_j , T_{stg}	-55...+175	°C
Soldering temperature, wave soldering only allowed at leads (1.6mm from case for 10s)	Tsold	260	°C

※. Notes:
1.EAS is tested at starting Tj = 25℃, L = 0.3mH, IAS =32A, VGS = 10V.

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Thermal Resistance

Parameter	Symbol	Max	Unit
Thermal resistance, junction – case.	R_{thJC}	1.21	°C/W
Thermal resistance, junction – ambient(min. footprint)	R_{thJA}	62	
Thermal resistance, junction – plastic case	R_{thJ-pc}	26	

Electrical Characteristic (at Tj = 25 °C, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Static Characteristic						
Drain-source breakdown voltage	BV_{DSS}	40	-	-	V	V_{GS}=0V, I_D=250uA
		40	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{GS(th)}$	1	-	3	V	V_{DS}=V_{GS},I_D=250uA
Zero gate voltage drain current	I_{DSS}	- -	- -	1 100	μA	V_{DS}=40V,V_{GS}=0V T_j=25°C T_j=125°C
Gate-source leakage current	I_{GSS}	-	-	±100	nA	V_{GS}=±20V,V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$		1.7	2.3	mΩ	VGS=10V, ID=50A
		-	2.5	4.0		VGS=4.5V, ID=50A
Transconductance	g_{fs}	94	187	374	S	VDS=5V, ID=50A
Dynamic Characteristic						
Input Capacitance	C_{iss}	1200	2600	5200	pF	VGS=0V, VDS=20V, f=1MHz
Output Capacitance	C_{oss}	450	960	1920		
Reverse Transfer Capacitance	C_{rss}	7	36	100		
Gate Total Charge	Q_G	28	42	63	nC	VGS=10V, VDS=20V, ID=50A, f=1MHz
Gate-Source charge	Q_{gs}	-	10.0	20		
Gate-Drain charge	Q_{gd}	-	7.0	14		
Turn-on delay time	$t_{d(on)}$	5	9	18	ns	Vds=20V Id=50A Rg=3Ω Vgs=10V
Rise time	t_r	-	24	48		
Turn-off delay time	$t_{d(off)}$	21	32	48		
Fall time	t_f	-	11	31.5		
Gate resistance	R_G	-	1.3	5	Ω	V_{GS}=0V, V_{DS}=0V, f=1MHz

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Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Diode continous forward current	Is	-	-	140	A	Tc = 25°C
Diode pulse current	Is pulse	-	-	560	A	Tc = 25°C
Body Diode Forward Voltage	V_{SD}	-	0.84	1.4	V	VGS=0V, ISD=50A
Body Diode Reverse Recovery Time	t_{rr}	18	35	70	ns	IF=50A,dI/dt=100A/μs
Body Diode Reverse Recovery Charge	Q_{rr}	13	25	50	nC	

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Typical Performance Characteristics

Fig 1: Output Characteristics

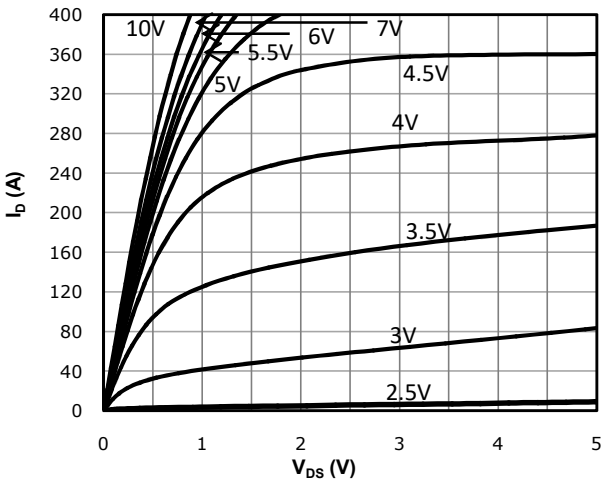


Fig 2: Transfer Characteristics

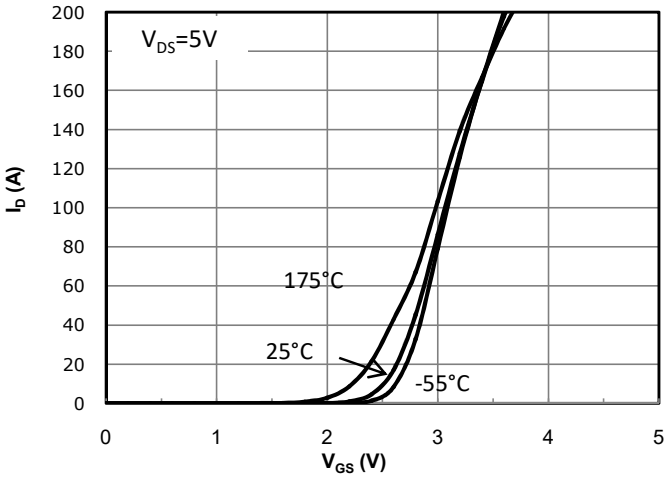


Fig 3: Rds(on) vs Drain Current and Gate Voltage

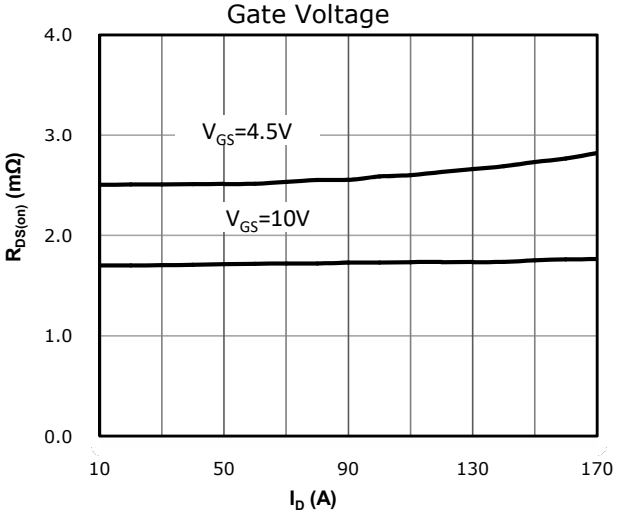


Fig 4: Rds(on) vs Gate Voltage

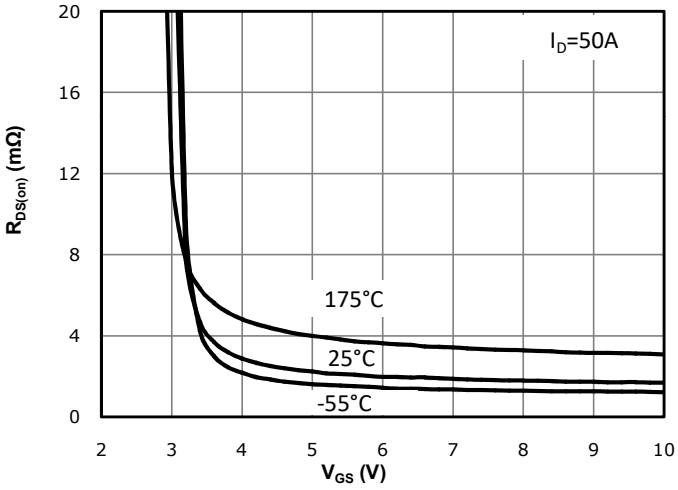


Fig 5: Rds(on) vs. Temperature

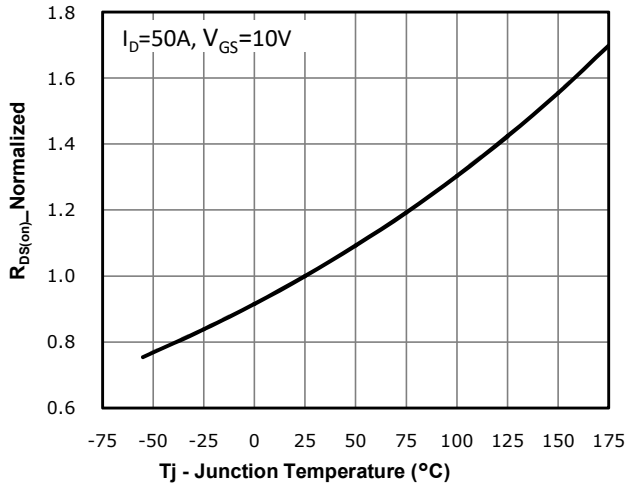
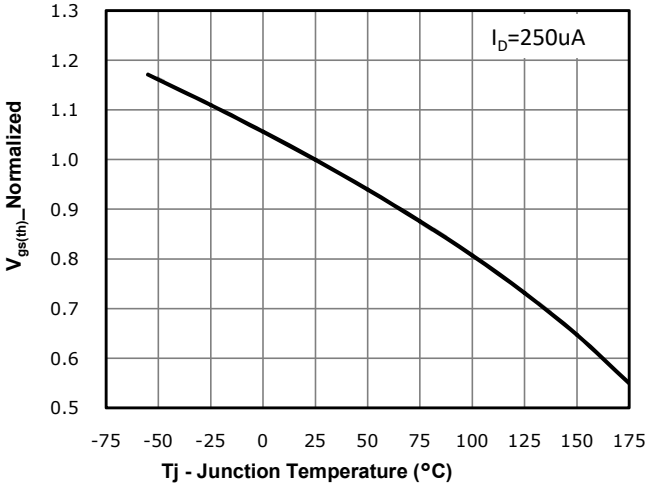


Fig 6: Vgs(th) vs. Temperature



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Fig 7: BVdss vs. Temperature

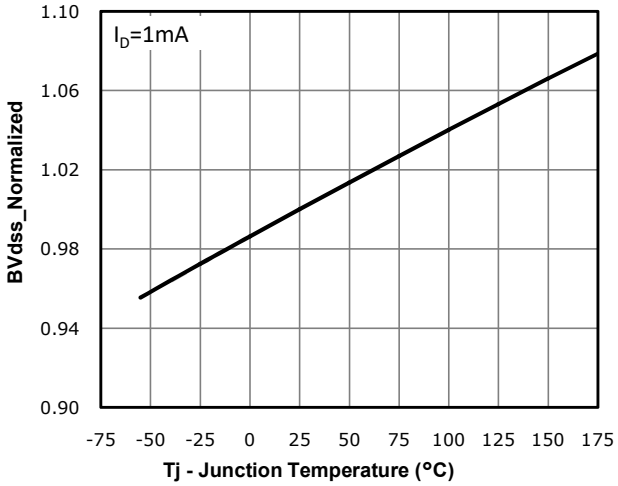


Fig 8: Capacitance Characteristics

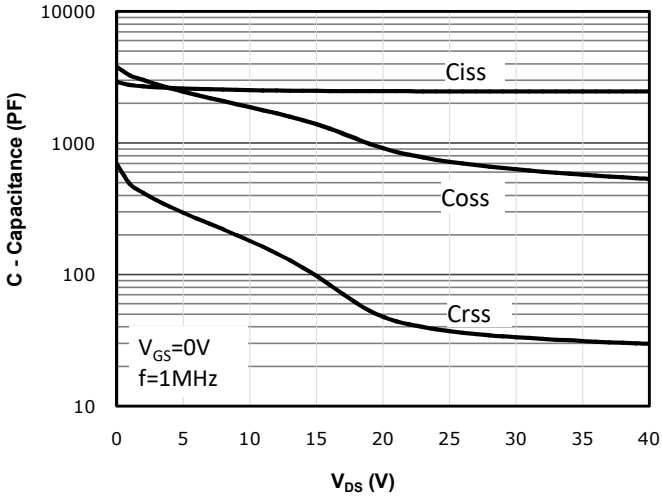


Fig 9: Gate Charge Characteristics

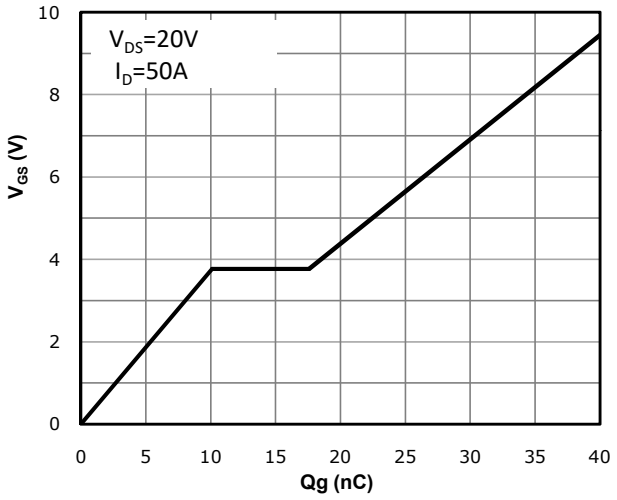


Fig 10: Body-diode Forward Characteristics

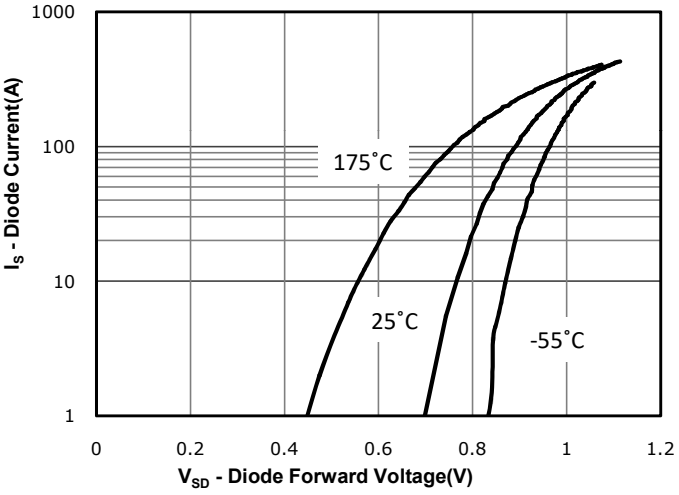


Fig 11: Power Dissipation

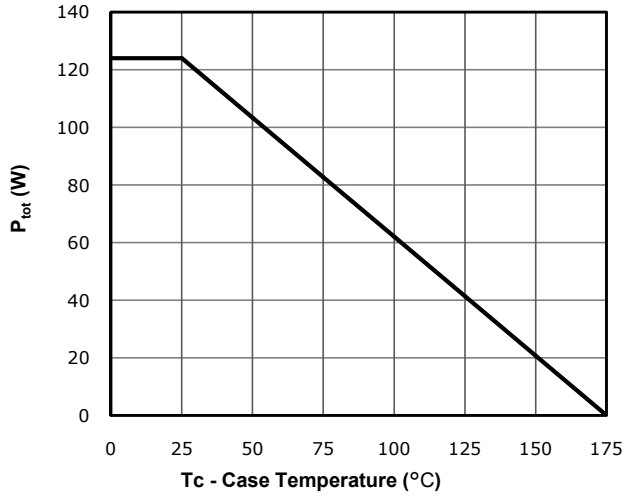
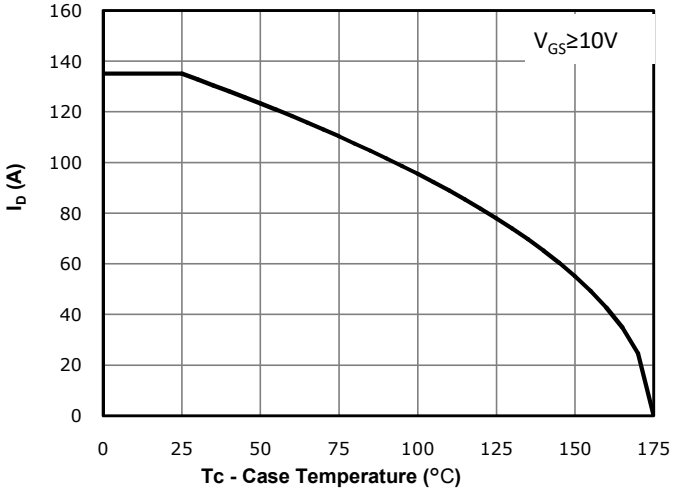


Fig 12: Drain Current Derating



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Fig 13: Safe Operating Area

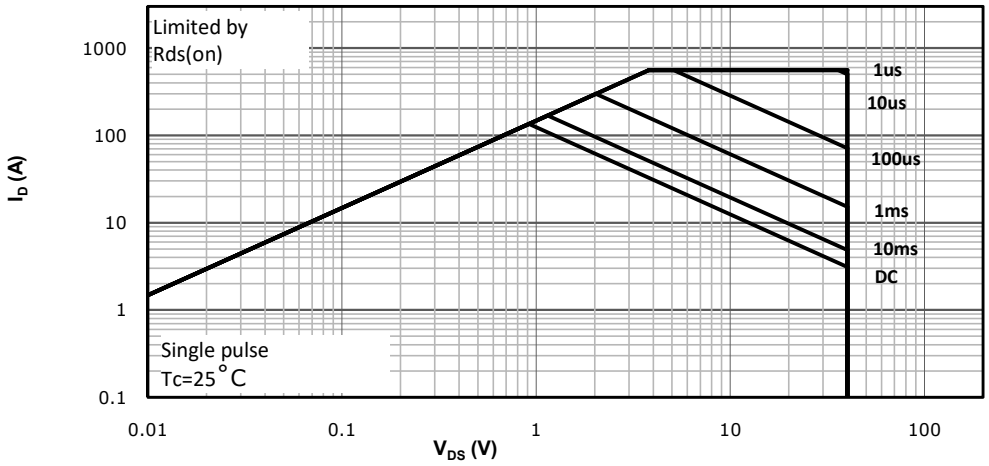
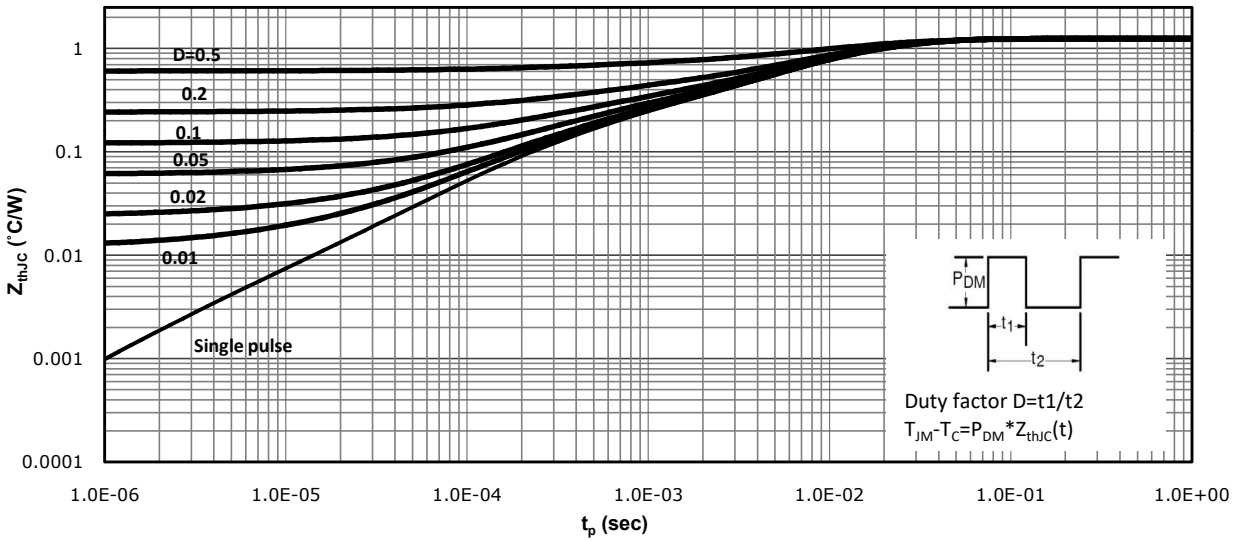


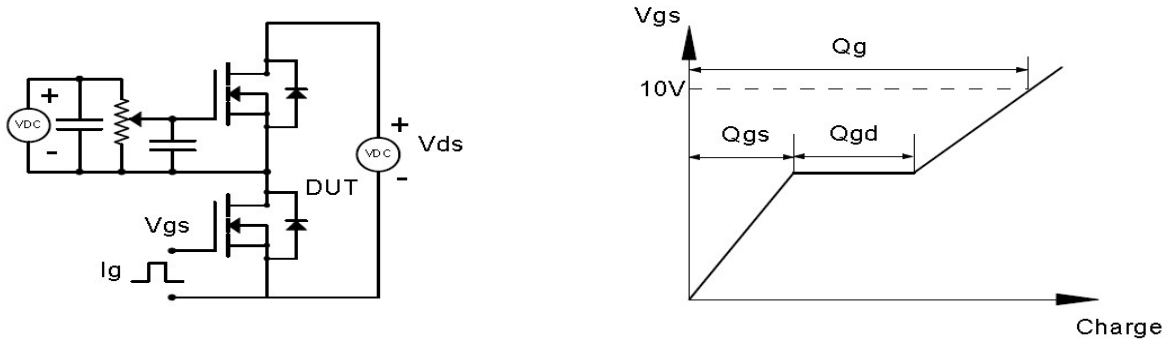
Fig 14: Max. Transient Thermal Impedance



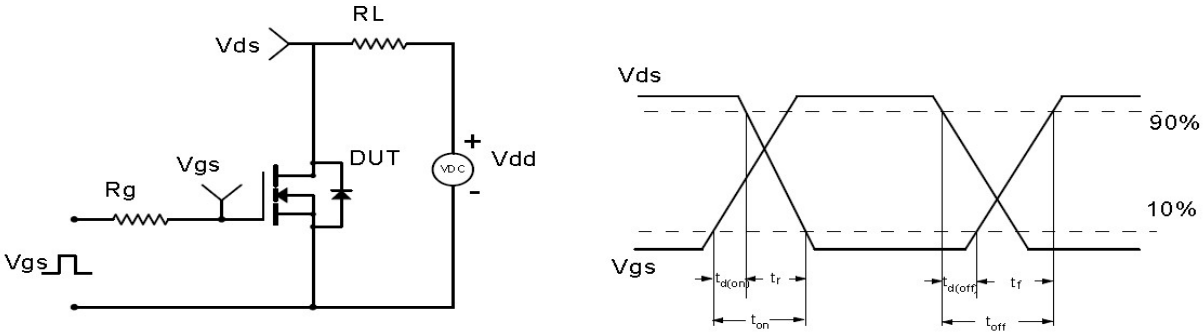
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Test Circuit & Waveform

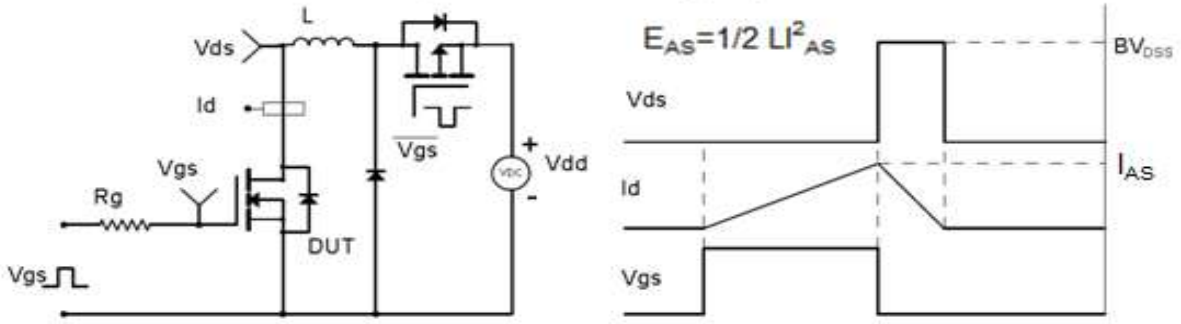
Gate Charge Test Circuit & Waveform



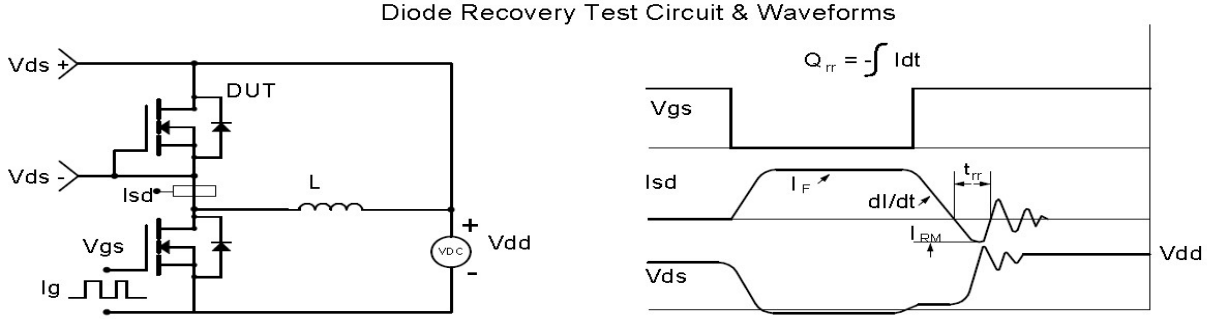
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

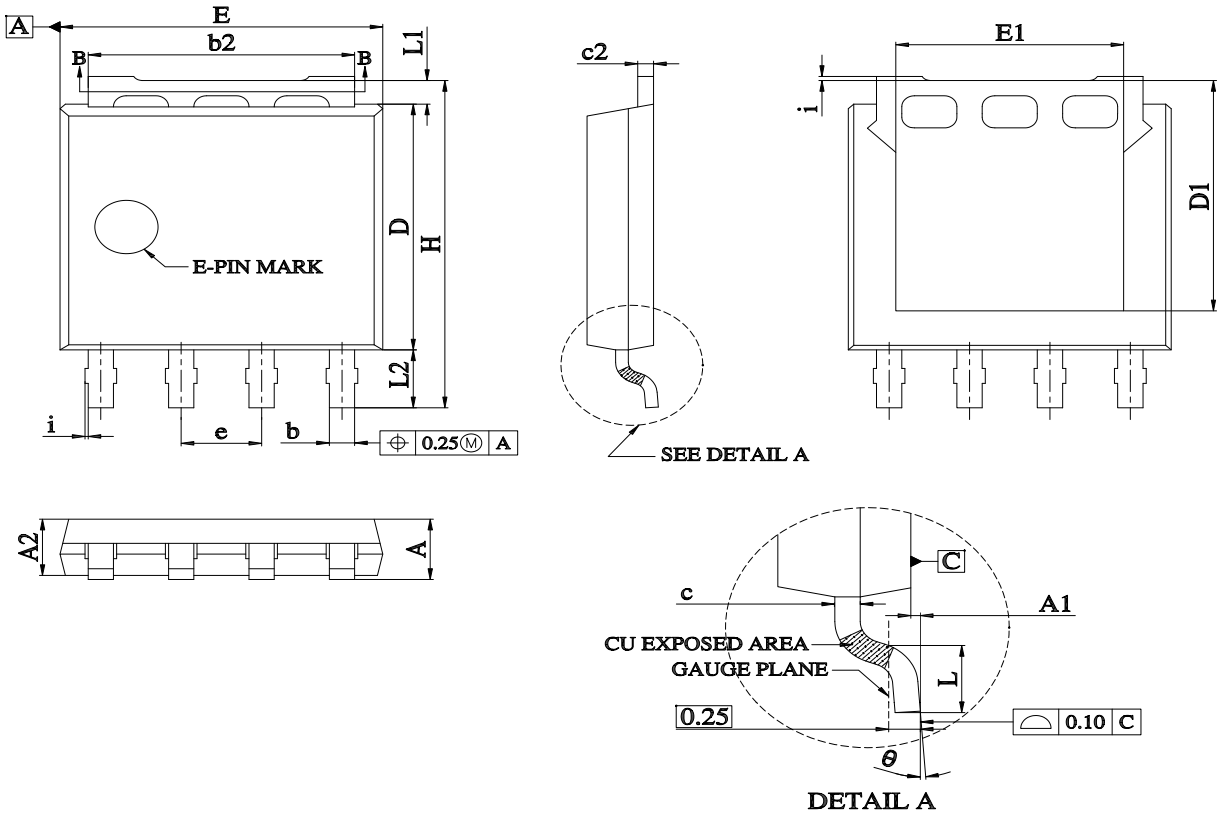


Diode Recovery Test Circuit & Waveforms



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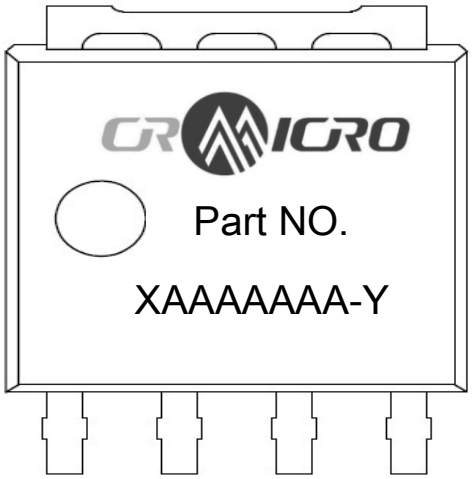
Package Outline: LFPAK5*6



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.00	1.20	0.039	0.047
A1	0.00	0.15	0.000	0.006
A2	0.95	1.15	0.037	0.045
b	0.32	0.50	0.013	0.020
b2	3.80	4.41	0.150	0.174
c	0.17	0.25	0.007	0.010
c2	0.22	0.30	0.009	0.012
D	4.45	4.70	0.175	0.185
D1	--	4.45	--	0.175
E	4.90	5.30	0.193	0.209
E1	3.45	3.75	0.136	0.148
e	1.27 BSC		0.050 BSC	
H	5.95	6.25	0.234	0.246
i	--	0.25	--	0.010
L	0.40	0.85	0.016	0.033
L1	0.27	0.57	0.011	0.022
L2	0.80	1.30	0.031	0.051
θ	0°	8°	0°	8°

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Marking



NOTE:
XAAAAAAA-Y
X —Assembly location code
AAAAAAA —Assembly lot NO. last 7digits
Y —Bin code

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Revision History

Revision	Date	Major changes
1.0	2023/9/5	Release of preliminary version.
1.1	2023/11/3	Update package outline
1.2	2023/12/21	Update marking
1.3	2024/4/28	Update Ciss Crss Coss spec；Add Is、 Is pulse；

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