General Description：

CS10N80A8HD, the silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-220, which accords with the RoHS standard.

V_{DSS}	800	V
I_D	10	A
P_D(T_C=25℃)	160	W
$R_{DS(ON)Typ}$	0.72	Ω

TO-220

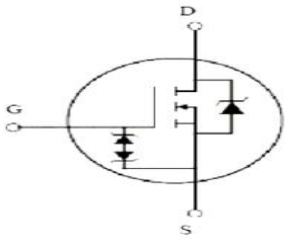


1.Gate 2. Drain 3. Source

Features：

- Fast Switching
- ESD Improved Capability
- Low Gate Charge (Typical Data:65 nC)
- Low Reverse transfer capacitances(Typical:25pF)
- 100% Single Pulse avalanche energy Test

Inner Equivalent Principium Chart



Applications：

Power switch circuit of PC POWER.

Absolute（Tc= 25℃ unless otherwise specified）:

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	800	V
I_D	Continuous Drain Current	10	A
	Continuous Drain Current T_C = 100 °C	6.5	A
I_{DM} [a1]	Pulsed Drain Current	40	A
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Energy	997	mJ
E_{AR} [a1]	Avalanche Energy ,Repetitive	40	mJ
I_{AR} [a1]	Avalanche Current	2.8	A
dv/dt [a2]	Peak Diode Recovery dv/dt	5.0	V/ns
P_D	Power Dissipation	160	W
	Derating Factor above 25°C	1.28	W/℃
$V_{ESD(G-S)}$	Gate source ESD (HBM-C= 100pF, R=1.5kΩ)	4000	V
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150，–55 to 150	℃
T_L	Maximum Temperature for Soldering	300	℃

Electrical Characteristics（T_C= 25℃ unless otherwise specified）:

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	800	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Bvdss Temperature Coefficient	ID=250uA, Reference25℃	--	0.5	--	V/℃
I_{DSS}	Drain to Source Leakage Current	V_{DS} =800V, V_{GS}= 0V, T_a = 25℃	--	--	25	μA
		V_{DS} =640V, V_{GS}= 0V, T_a= 125℃	--	--	250	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS} =+20V	--	--	10	μA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS} =-20V	--	--	-10	μA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}=10V,I_D=5A	--	0.72	0.9	Ω
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D = 250μA	2.0	--	4.0	V
Pulse width tp≤300μs,δ≤2%						

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g_{fs}	Forward Trans conductance	V_{DS}=15V, I_D =10A	--	20	--	S
C_{iss}	Input Capacitance	V_{GS} = 0V V_{DS} = 25V f = 1.0MHz	--	2900	--	pF
C_{oss}	Output Capacitance		--	200	--	
C_{rss}	Reverse Transfer Capacitance		--	25	--	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	I_D =10A V_{DD} = 400V V_{GS} = 10V R_G =4.7Ω	--	19	--	ns
tr	Rise Time		--	10	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	68	--	
t_f	Fall Time		--	23	--	
Q_g	Total Gate Charge	I_D =10A V_{DD} =640V V_{GS} = 10V	--	65	--	nC
Q_{gs}	Gate to Source Charge		--	13	--	
Q_{gd}	Gate to Drain (“Miller”)Charge		--	25	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)		--	--	10	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	40	A
V_{SD}	Diode Forward Voltage	I_S=10A,V_{GS}=0V	--	--	1.5	V
trr	Reverse Recovery Time	I_S=10A,T_j= 25℃	--	200	--	ns
Qrr	Reverse Recovery Charge	dI_F/dt=100A/us, V_{GS}=0V	--	2.2	--	μC
Pulse width tp≤300μs,δ≤2%						

Symbol	Parameter	Typ.	Units
$R_{\theta JC}$	Junction-to-Case	0.78	℃/W
$R_{\theta JA}$	Junction-to-Ambient	62.5	℃/W

Gate-source Zener diode						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{GSO}	Gate-source breakdown voltage	I_{GS}=±1mA(Open Drain)	30			V
The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.						

[a1]: Repetitive rating; pulse width limited by maximum junction temperature
[a2]: I_{SD} =9A,di/dt ≤100A/us,V_{DD}≤$BV_{DS,}$ Start T_J=25℃

Characteristics Curve：

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

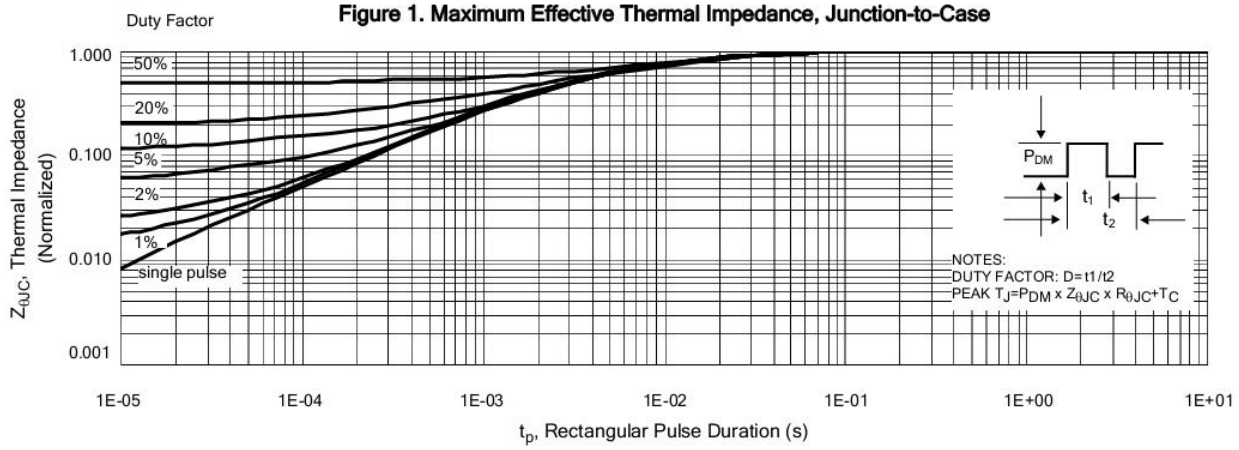


Figure 2. Maximum Power Dissipation vs Case Temperature

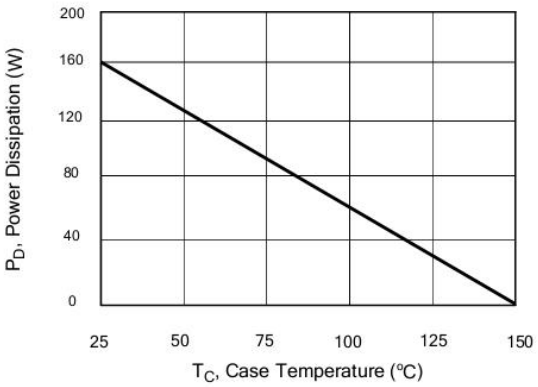


Figure3. Maximum Continuous Drain Current vs Case Temperature

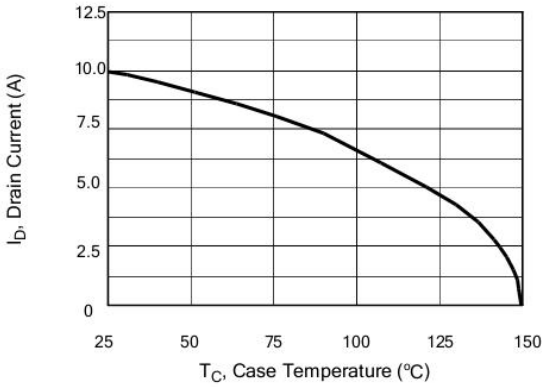


Figure 4. Typical Output Characteristics

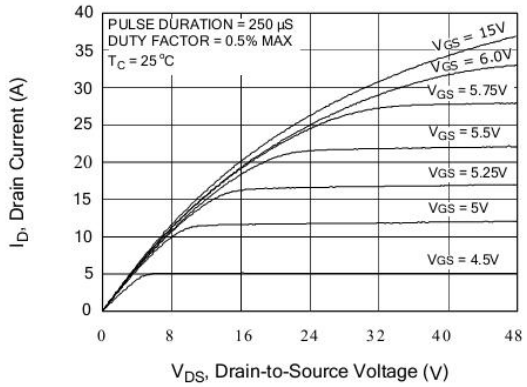


Figure5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current

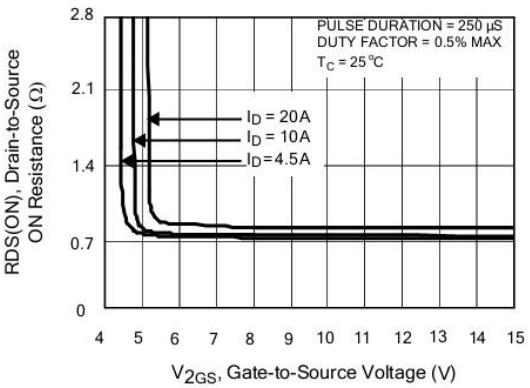


Figure 6. Maximum Peak Current Capability

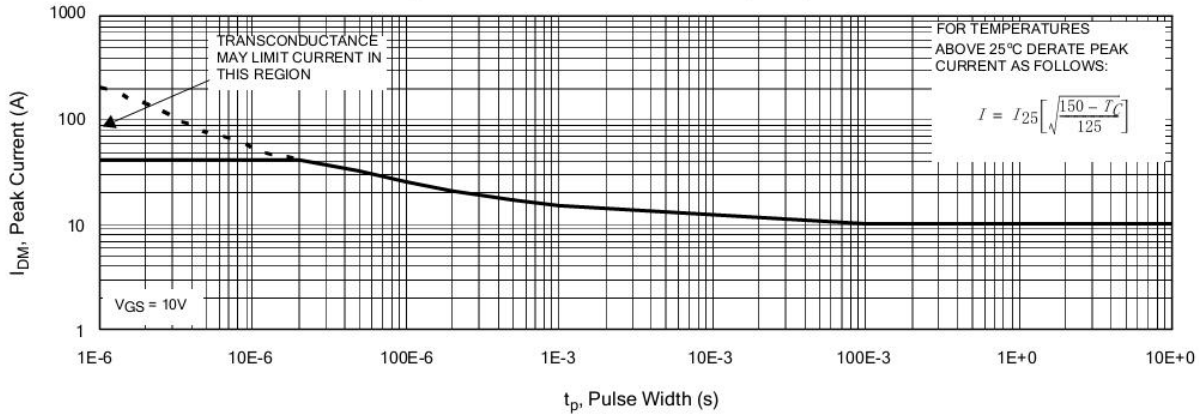


Figure 7. Typical Transfer Characteristics

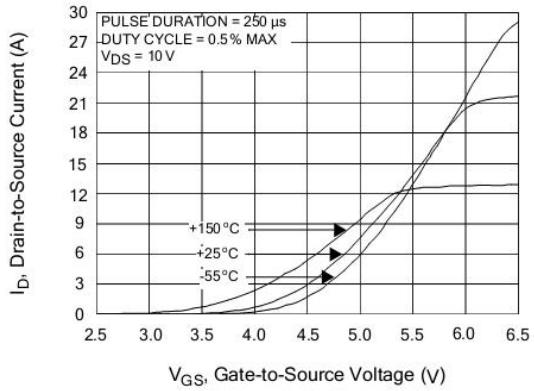


Figure8. Unclamped Inductive Switching Capability

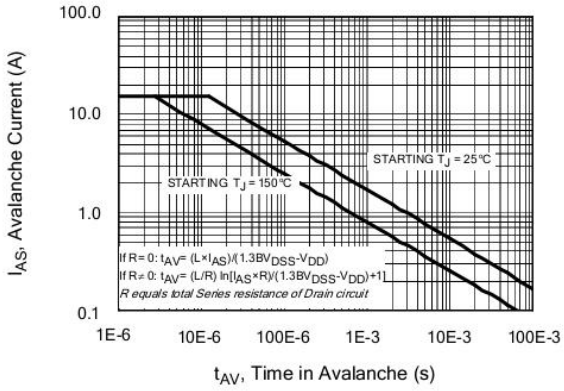


Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current

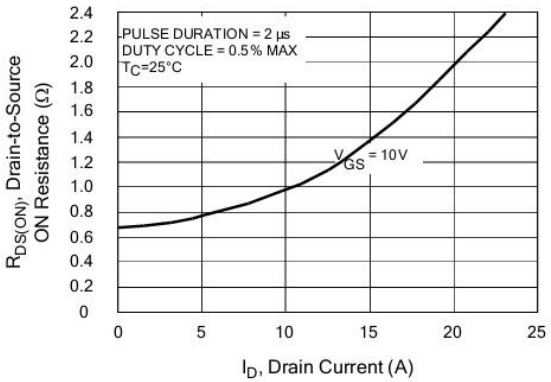


Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature

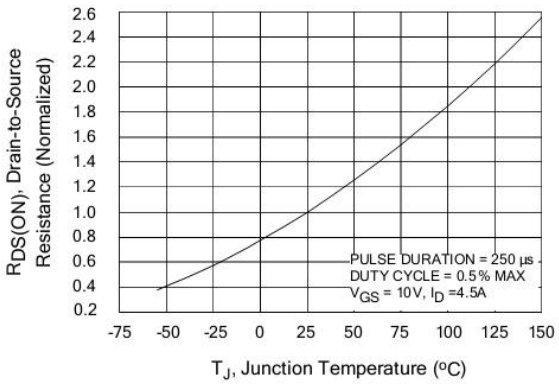


Figure 11. Typical Breakdown Voltage vs Junction Temperature

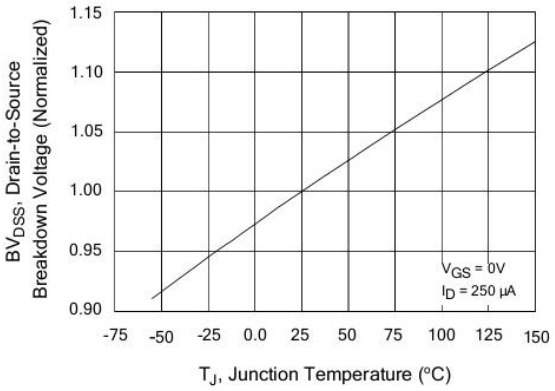


Figure 12. Typical Threshold Voltage vs Junction Temperature

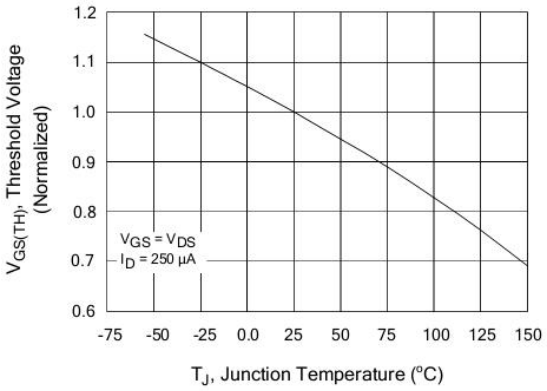


Figure 13. Maximum Forward Bias Safe Operating Area

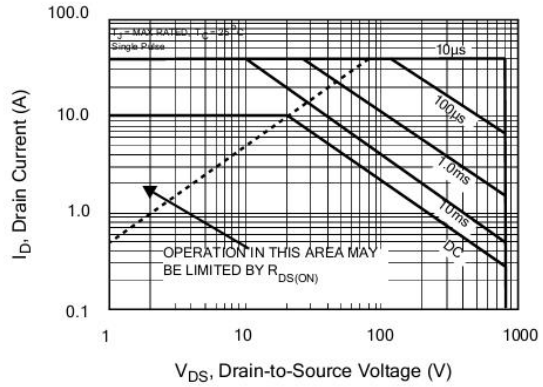


Figure 14. Typical Capacitance vs Drain-to-SourceVoltage

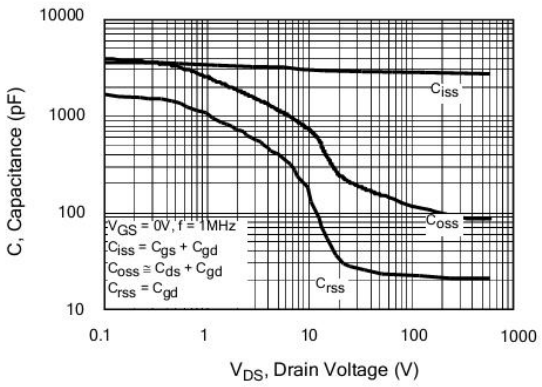


Figure 15. Typical Gate Charge vs Gate-to-Source Voltage

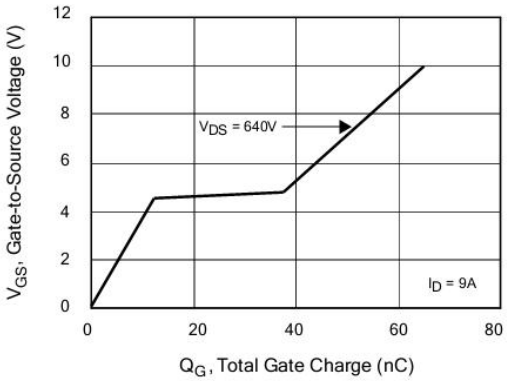
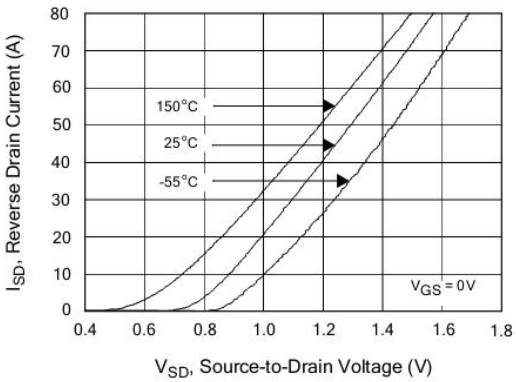


Figure 16. Typical Body Diode Transfer Characteristics



Test Circuit and Waveform：

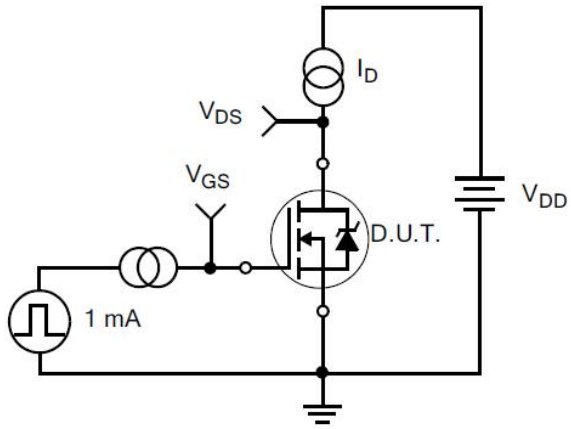


Figure 17. Gate Charge Test Circuit

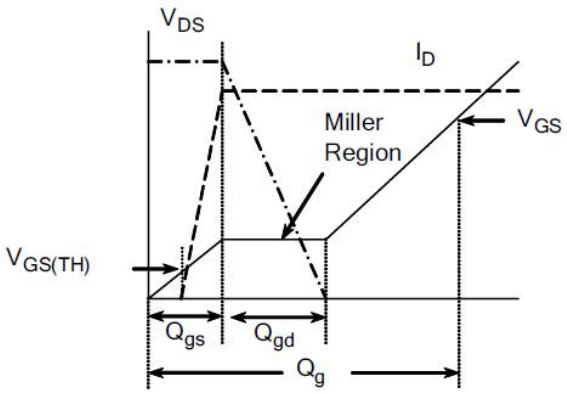


Figure 18. Gate Charge Waveforms

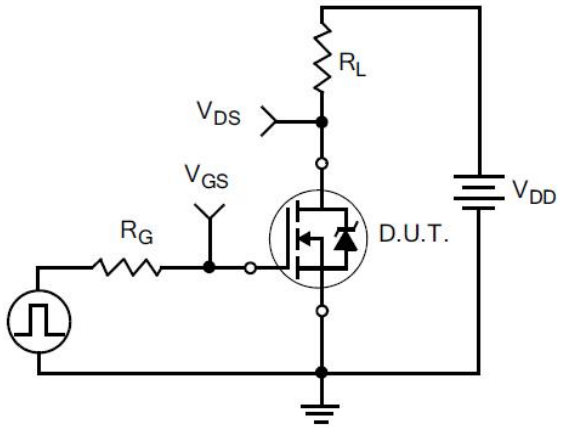


Figure 19. Resistive Switching Test Circuit

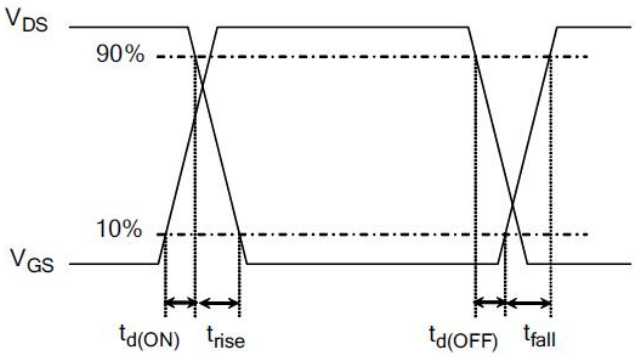


Figure 20. Resistive Switching Waveforms

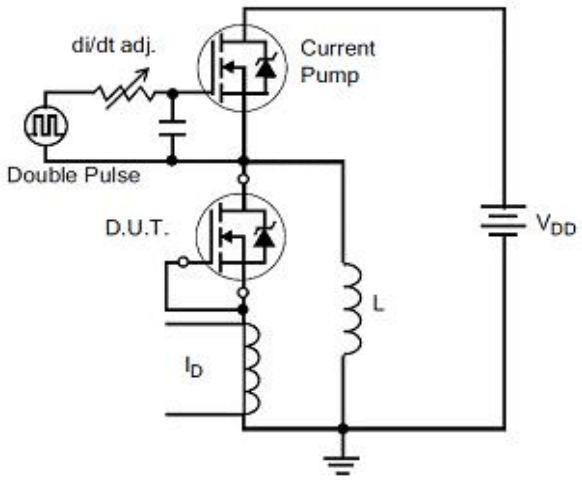


Figure 21. Diode Reverse Recovery Test Circuit

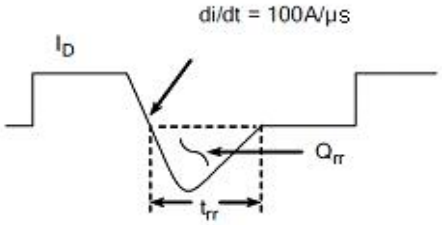


Figure 22. Diode Reverse Recovery Waveform

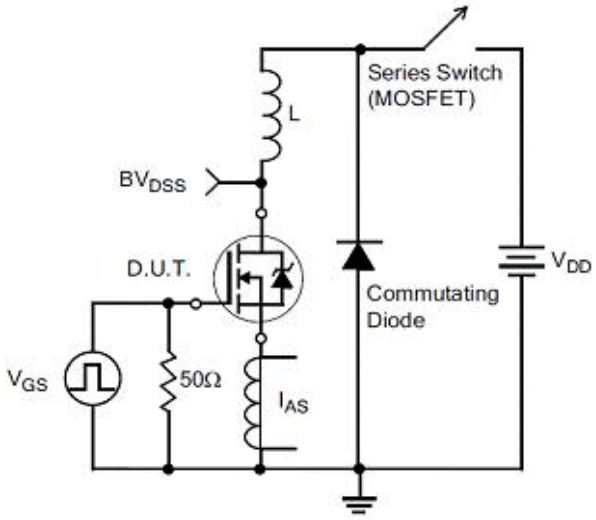


Figure23.Unclamped Inductive Switching Test Circuit

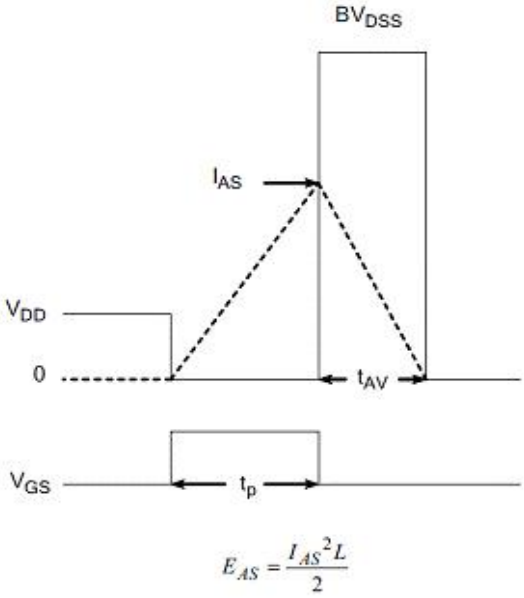
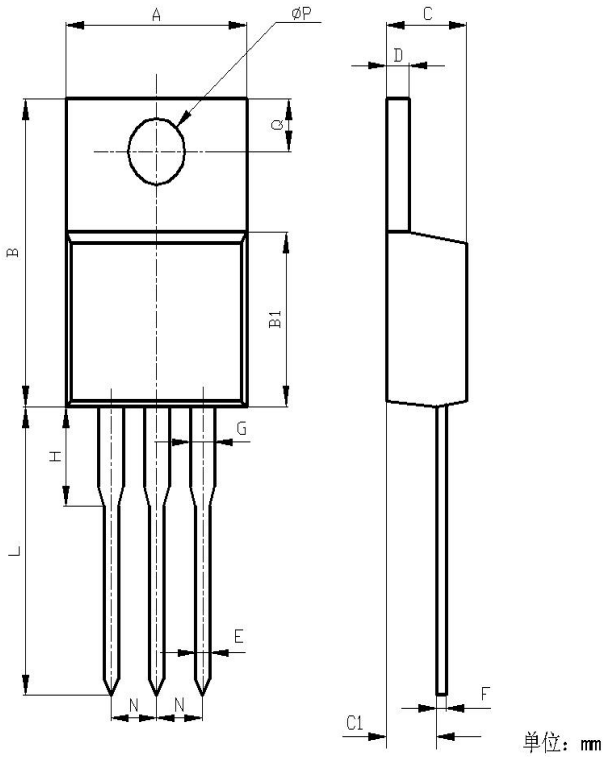


Figure24.Unclamped Inductive Switching Waveform

Package Information：



Items	Values(mm)	
	MIN	MAX
A	9.60	10.6
B	15.0	16.0
B1	8.90	9.50
C	4.30	4.80
C1	2.30	3.10
D	1.20	1.40
E	0.70	0.90
F	0.30	0.60
G	1.17	1.37
H	2.70	3.80
L	12.6	14.8
N	2.34	2.74
Q	2.40	3.00
ΦP	3.50	3.90

TO-220 Package

The name and content of poisonous and harmful material in products

	Hazardous Substance									
	Pb	Hg	Cd	Cr(VI)	PBB	PBDE	DIBP	DEHP	DBP	BBP
Limit	⩽ 0.1%	⩽ 0.1%	⩽ 0.01%	⩽ 0.1%	⩽ 0.1%	⩽ 0.1%	⩽ 0.1%	⩽ 0.1%	⩽ 0.1%	⩽ 0.1%
Lead Frame	○	○	○	○	○	○	○	○	○	○
Molding	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
Wire Bonding	○	○	○	○	○	○	○	○	○	○
Solder	×	○	○	○	○	○	○	○	○	○
Note	○: Means the hazardous material is under the criterion of 2011/65/EU. ×: Means the hazardous material exceeds the criterion of 2011/65/EU. The plumbum element of solder exist in products presently, but within the allowed range of Eurogroup's RoHS.									

Warnings

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. It is suggested to be used under 80 percent of the maximum ratings of the device.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. VDMOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. This publication is made by Huajing Microelectronics and subject to regular change without notice.

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Revison History		
Revision	Date	Major changes
1.0	2019/9/5	Initial release
2.0	2025/7/17	Change header and footer