Features

- Uses CRM(CQ) advanced SkyMOS2 technology
- Extremely low on-resistance $R_{DS(on)}$
- Excellent Q_gx$R_{DS(on)}$ product(FOM)
- Qualified according to JEDEC criteria

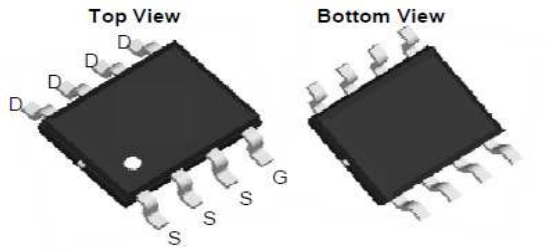
Product Summary

V_{DS}	100
$R_{DS(on)@10V\ typ}$	11.0mΩ
$R_{DS(on)@4.5V\ typ}$	14.0mΩ
I_D	11A

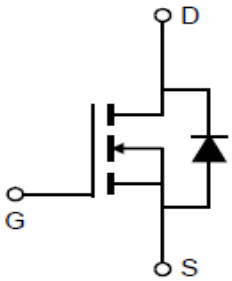
Applications

- Synchronous Rectification for AC/DC Quick Charger
- Battery management
- UPS (Uninterrupible Power Supplies)

100% Avalanche Tested



CRSE120N10L2



Package Marking and Ordering Information

Part #	Marking	Package	Packing	Reel Size	Tape Width	Qty
CRSE120N10L2	SE120N10L2	SOP-08	Tape&Reel	N/A	N/A	4000pcs

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	100	V
Continuous drain current T_A = 25°C T_A = 75°C	I_D	 11 8	A
Pulsed drain current (T_A = 25°C, t_p limited by T_{jmax})	$I_{D\ pulse}$	44	A
Avalanche energy, single pulse (L=0.1mH, Rg=25Ω)	E_{AS}	45	mJ
Gate-Source voltage	V_{GS}	±20	V
Power dissipation (T_A = 25°C)	P_{tot}	2.8	W
Operating junction and storage temperature	T_j , T_{stg}	-55...+150	°C

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Thermal Resistance

Parameter	Symbol	Max	Unit
Thermal resistance, junction – case.	R_{thJC}	21.8	°C/W
Thermal resistance, junction – ambient(min. footprint)	R_{thJA}	45	

Electrical Characteristic (at Tj = 25 °C, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Static Characteristic						
Drain-source breakdown voltage	BV_{DSS}	100	115	-	V	V_{GS}=0V, I_D=250uA
Gate threshold voltage	$V_{GS(th)}$	1.4	1.8	2.2	V	V_{DS}=V_{GS},I_D=250uA
Zero gate voltage drain current	I_{DSS}	- -	0.05 -	1 100	μA	V_{DS}=100V,V_{GS}=0V T_j=25°C T_j=125°C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=±20V,V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	-	11.0	13.2	mΩ	V_{GS}=10V, I_D=11A
		-	14.0	16.5		V_{GS}=4.5V, I_D=11A
Transconductance	g_{fs}	-	38	-	S	V_{DS}=5V,I_D=11A
Dynamic Characteristic						
Input Capacitance	C_{iss}	-	1618	-	pF	V_{GS}=0V, V_{DS}=50V, f=1MHz
Output Capacitance	C_{oss}	-	277	-		
Reverse Transfer Capacitance	C_{rss}	-	22	-		
Gate Total Charge	Q_G	-	28.2	-	nC	V_{GS}=10V, V_{DS}=50V, I_D=11A, f=1MHz
Gate-Source charge	Q_{gs}	-	6.5	-		
Gate-Drain charge	Q_{gd}	-	4.5	-		
Turn-on delay time	$t_{d(on)}$	-	30	-	ns	V_{GS}=10V, V_{DD}=50V, R_{G_ext}=2.7Ω
Rise time	t_r	-	81	-		
Turn-off delay time	$t_{d(off)}$	-	24	-		
Fall time	t_f	-	7	-		
Gate resistance	R_G	-	1.62	-	Ω	V_{GS}=0V, V_{DS}=0V, f=1MHz

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Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	-	0.83	1	V	V_{GS}=0V,I_{SD}=11A
Body Diode Reverse Recovery Time	t_{rr}	-	78	-	ns	I_F=11A, dI/dt=100A/μs
Body Diode Reverse Recovery Charge	Q_{rr}	-	192	-	nC	

Typical Performance Characteristics

Fig 1: Output Characteristics

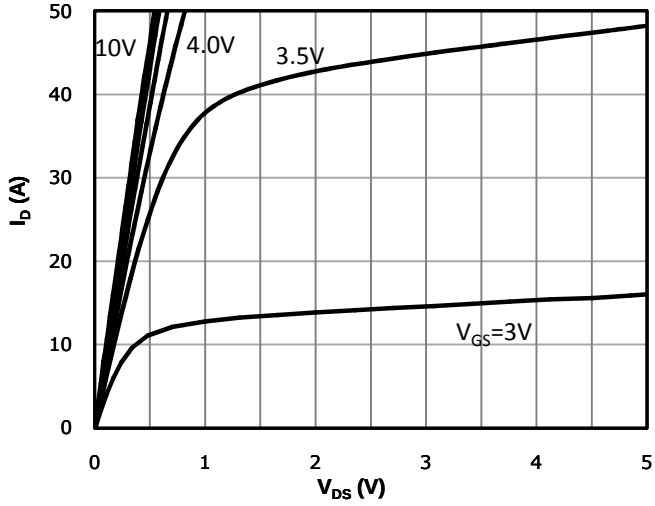


Fig 2: Transfer Characteristics

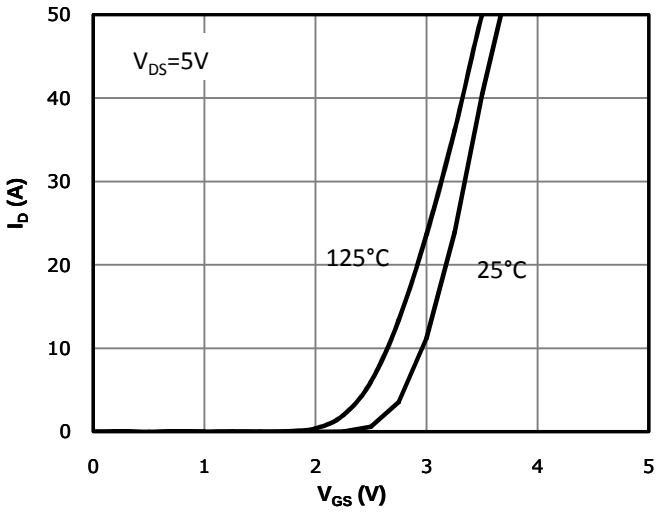


Fig 3: Rds(on) vs Drain Current and Gate Voltage

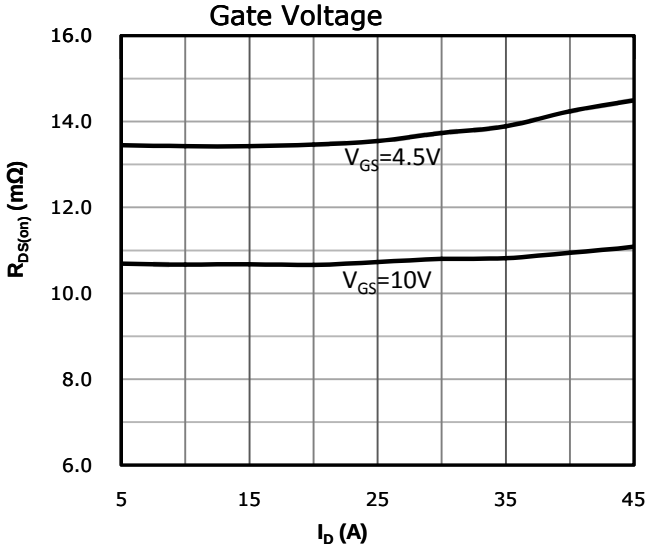


Fig 4: Rds(on) vs Gate Voltage

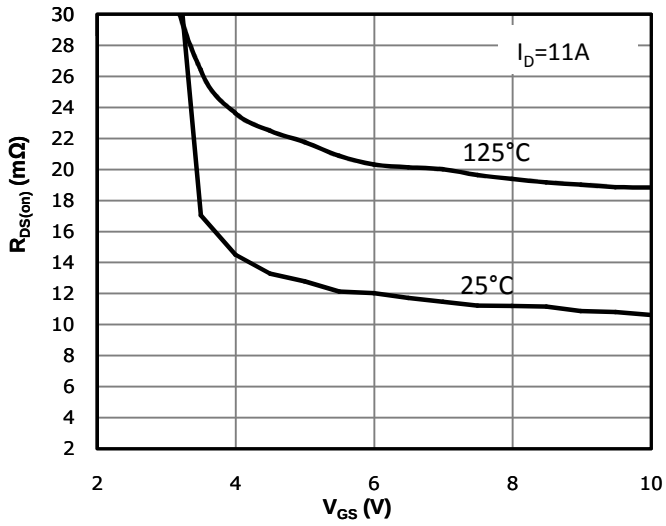


Fig 5: Rds(on) vs. Temperature

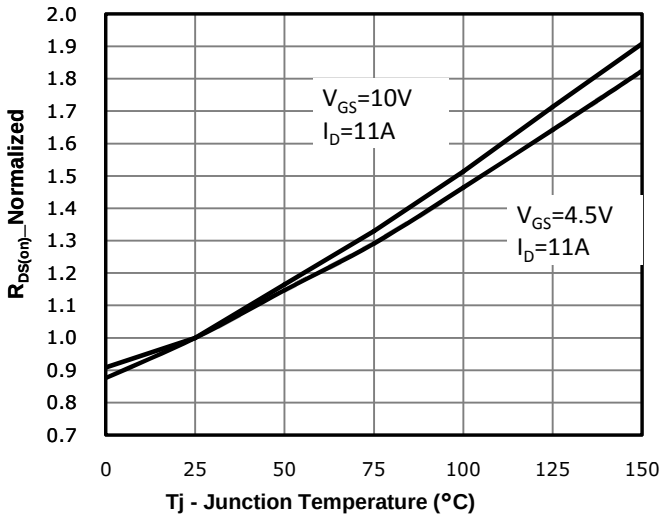


Fig 6: Capacitance Characteristics

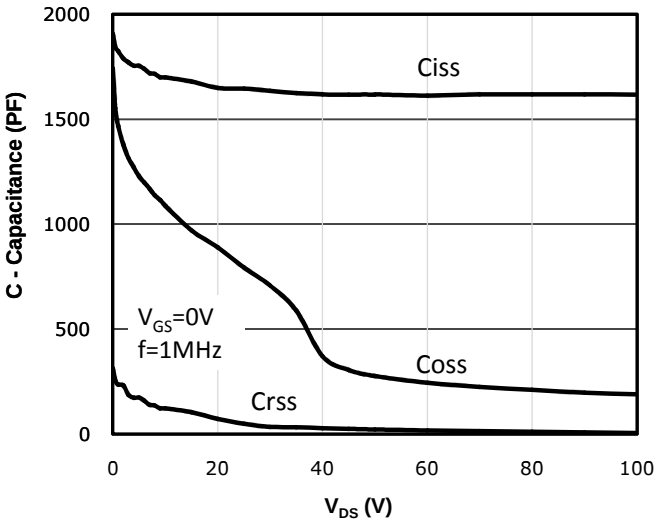


Fig 7: Gate Charge Characteristics

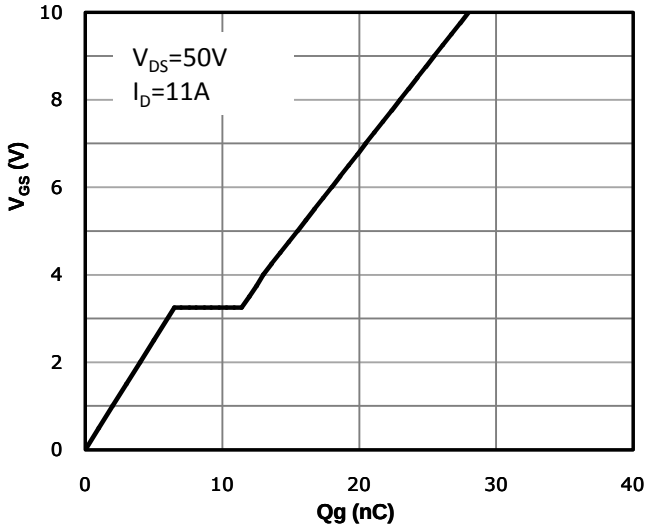


Fig 8: Body-diode Forward Characteristics

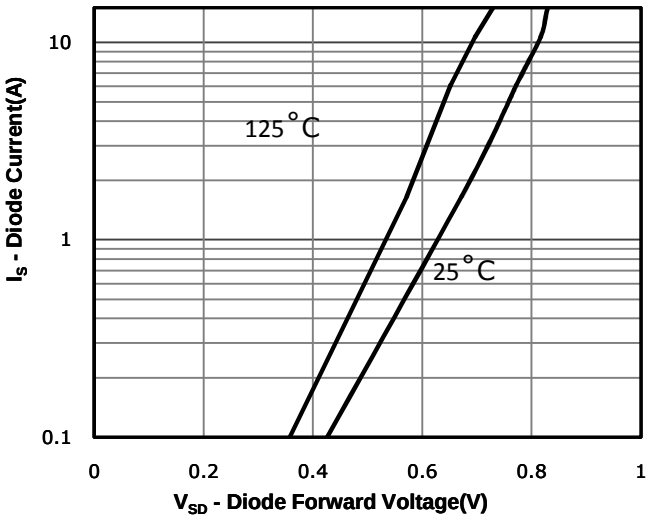


Fig 9: Power Dissipation

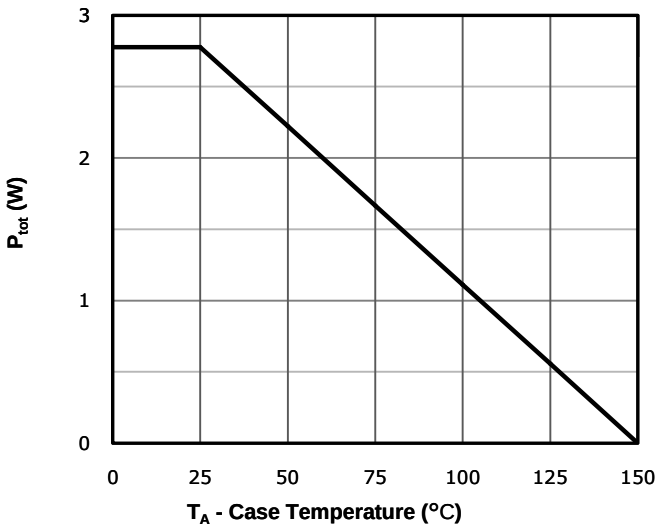


Fig 10: Drain Current Derating

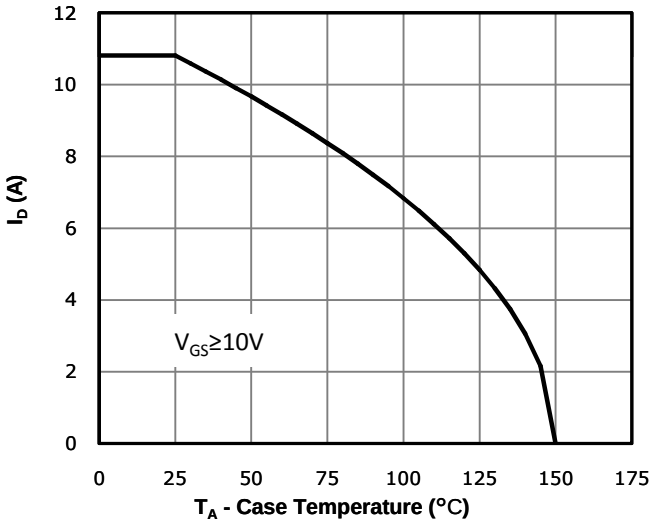


Fig 11: Safe Operating Area

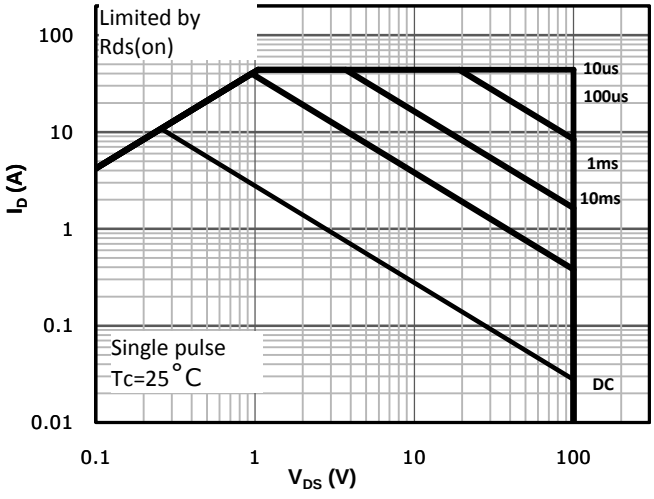
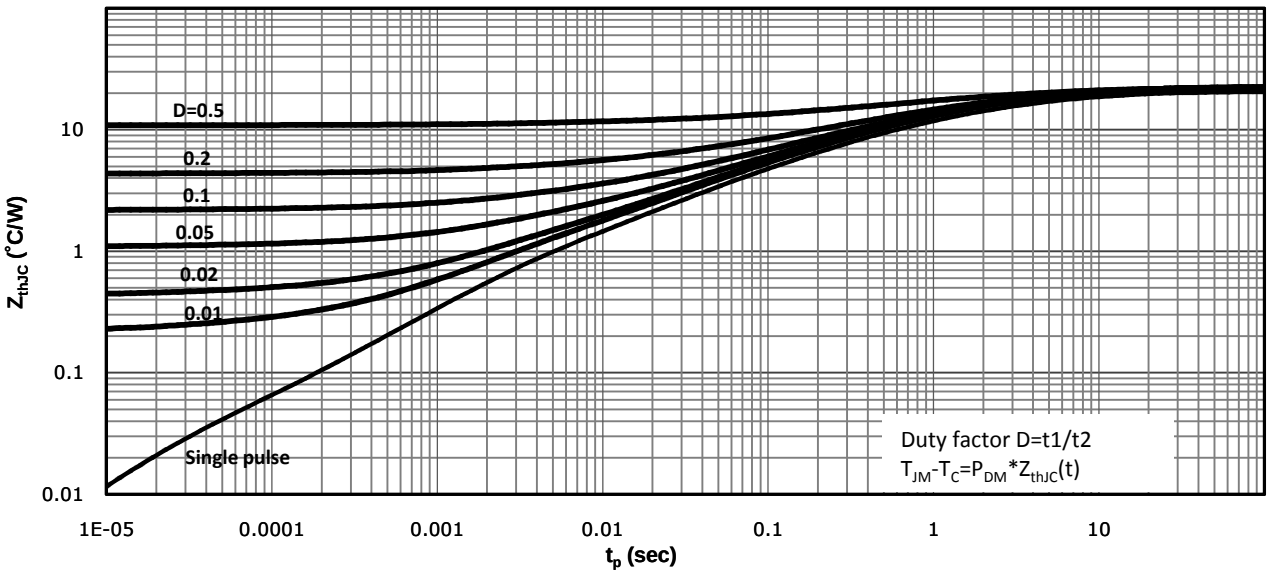
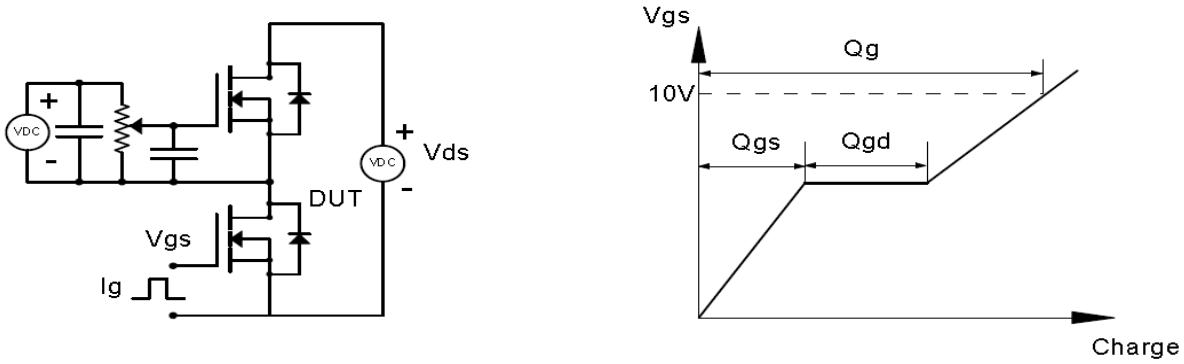


Fig 12: Max. Transient Thermal Impedance

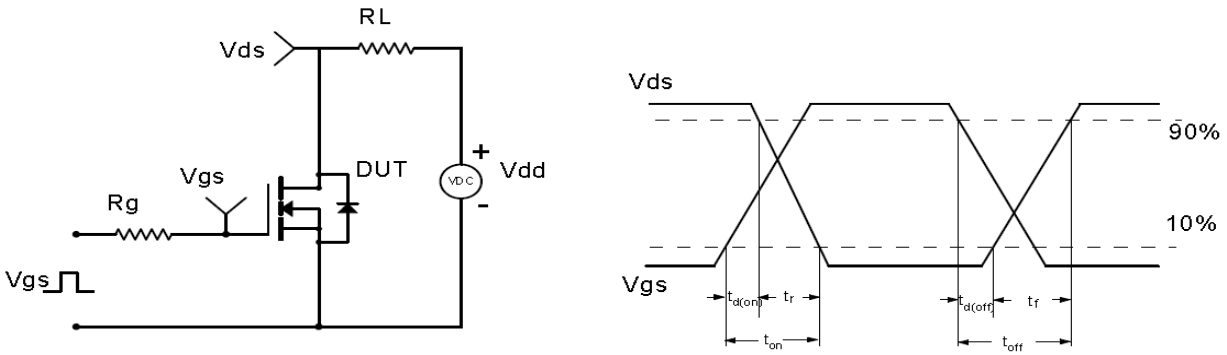


Test Circuit & Waveform

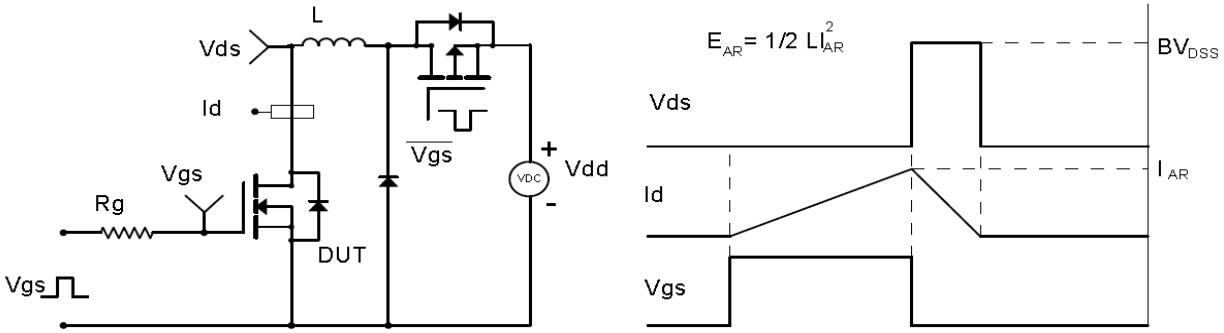
Gate Charge Test Circuit & Waveform



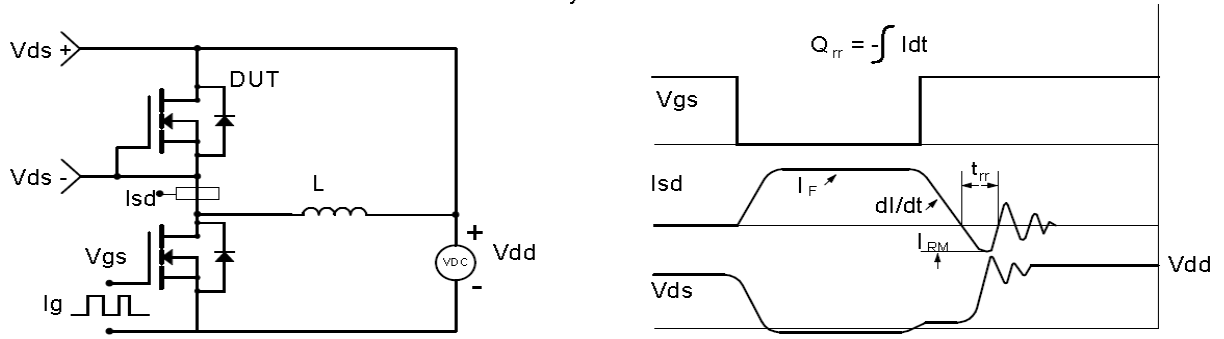
Resistive Switching Test Circuit & Waveforms



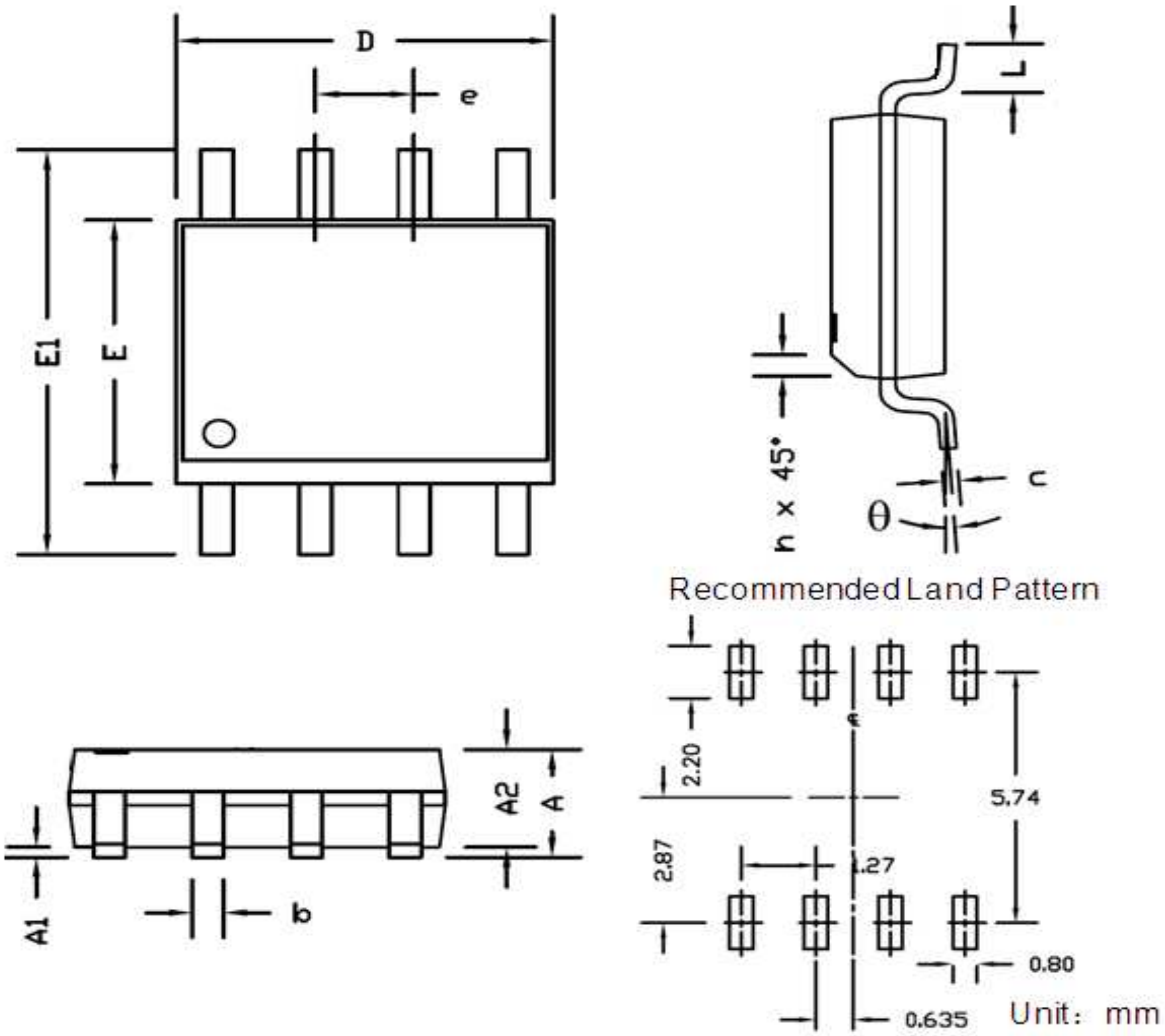
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Package Outline: SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.65	0.049	0.065
b	0.33	0.51	0.013	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
e	1.27 BSC.		0.050 BSC.	
E	3.80	4.00	0.150	0.157
E1	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

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Marking



NOTE:
XBBAAAAY

X	—Assembly location code
BB	—Fab code
AAAA	—Lot code
Y	—Bin code

Revision History

Revison	Date	Major changes
1.0	2018-4-12	priliminary version.
2.0	2019-7-4	Supplement package outline info.
3.0	2019-12-16	Supplement Marking rule info.

Disclaimer

Unless otherwise specified in the datasheet, the product is designed and qulified as a standard commercial product and is not intended for use in applications that require extraordinary levels of quality and reliability, such as automotive, aviation/aerospace and life-support devices or systems.

Any and all semicondutor products have certain probability to fail or malfunction, which may result in personal injury, death or property damage. Customer are solely responsible for providing adequate safe measures when design their systems.

CRM(CQ) reserves the right to improve product design, function and reliability without notice.