CRJL125N65G2BF

SJMOS N-MOSFET 650V, 109mΩ, 18A

Features

- CRM(CQ) Super_Junction technology
- Much lower Ron*A performance for On-state efficiency
- Better efficiency due to very low FOM
- Ultra-fast body diode
- Qualified for industrial grade applications according to JEDEC

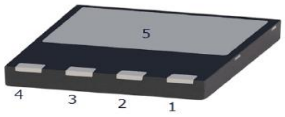
Product Summary

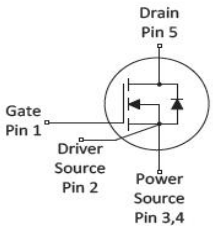
V_{DS}	650V
$R_{DS(on),typ}$	109mΩ
I_D	18A

Applications

- LED/LCD/PDP TV and monitor Lighting
- Solar/Renewable/UPS -Micro Inverter System
- Charger
- Power Supply

100% DVDS Tested
100% Avalanche Tested





Package Marking and Ordering Information

Part #	Marking	Package	Packing	Reel Size	Tape Width	Qty
CRJL125N65G2BF	CRJL125N65G2BF	DFN8*8	Tape&Reel	N/A	N/A	3000pcs

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	650	V
Continuous drain current [1)] T_C = 25℃ T_C = 100℃	I_D	 18 12	A
Pulsed drain current [2)] (T_C = 25℃, t_p limited by $T_{j,max}$)	$I_{D,pulse}$	55	A
Avalanche energy, single pulse (L=30mH)	E_{AS}	300	mJ
MOSFET dv/dt ruggedness	dv/dt	50	V/ns
Gate-Source voltage	V_{GS}	±30	V
Power dissipation (T_C = 25℃)	P_{tot}	89	W
Continuous diode forward current(T_C = 25℃)	I_S	18	A
Diode pulse current [2)] (T_C = 25°C)	$I_{S,pulse}$	55	A
Recovery diode dv/dt [3)]	dv/dt	50	V/ns
Operating junction and storage temperature	T_j , T_{stg}	-55...+150	℃

1) Limited by $T_{j,max}$. Maximum Duty Cycle D = 0.50
2) Pulse width t_p limited by $T_{j,max}$
3) Identical low side and high side switch with identical R_g

Thermal Resistance

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Thermal resistance, junction – case	R_{thJC}	-	1.00	1.40	℃/W	
Thermal resistance, junction – ambient	R_{thJA}	-	-	56	℃/W	

Electrical Characteristic (at T_j = 25 ° C, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Static Characteristic						
Drain-source breakdown voltage	BV_{DSS}	650	-	-	V	V_{GS}=0V,I_D=250μA
Gate threshold voltage	$V_{GS(th)}$	3.2	-	4.6	V	V_{DS}=V_{GS},I_D=250μA
Zero gate voltage drain current	I_{DSS}	- -	- 700	5 -	μA	V_{DS}=650V,V_{GS}=0V T_j=25℃ T_j=150℃
Gate-source leakage current	I_{GSS}	-	-	±100	nA	V_{GS}=±30V,V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	109 250	125 -	mΩ	V_{GS}=10V,I_D=12A, T_j=25℃ T_j=150℃
Transconductance	g_{fs}	-	17	-	S	V_{DS}=20V,I_D=12A
Dynamic Characteristic						
Input Capacitance	C_{iss}	-	1580	-	pF	V_{GS}=0V, V_{DS}=100V, f=100kHz
Output Capacitance	C_{oss}	-	88	-		
Reverse Transfer Capacitance	C_{rss}	-	1.2	-		
Gate Total Charge	Q_g	-	52	-	nC	V_{GS}=10V, V_{DS}=480V, I_D=12A
Gate-Source charge	Q_{gs}	-	14	-		
Gate-Drain charge	Q_{gd}	-	30	-		
Gate plateau voltage	$V_{plateau}$	-	7.6	-	V	
Turn-on delay time	$t_{d(on)}$	-	25	-	ns	V_{GS}=10V, I_D=12A, V_{DS}=400V, R_g=2Ω
Rise time	t_r	-	50	-		
Turn-off delay time	$t_{d(off)}$	-	65	-		
Fall time	t_f	-	28	-		
Gate resistance	$R_{g,int}$	-	9	-	Ω	f=1MHz

Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	0.7	0.9	1.1	V	V_{GS}=0V,I_{SD}=12A
Body Diode Reverse Recovery Time	t_{rr}	-	97	-	ns	I_{SD}=12A di_F/dt=100A/μs V_{DS}=400V
Body Diode Reverse Recovery Charge	Q_{rr}	-	0.4	-	μC	
Body Diode Reverse Recovery Peak Current	I_{rrm}	-	7.5	-	A	

Typical Performance Characteristics

Fig 1. Output Characteristics (T_j=25℃)

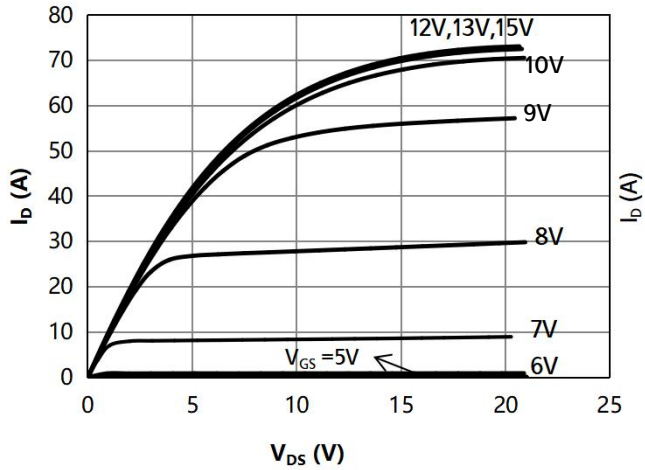


Fig 2. Output Characteristics (T_j=150℃)

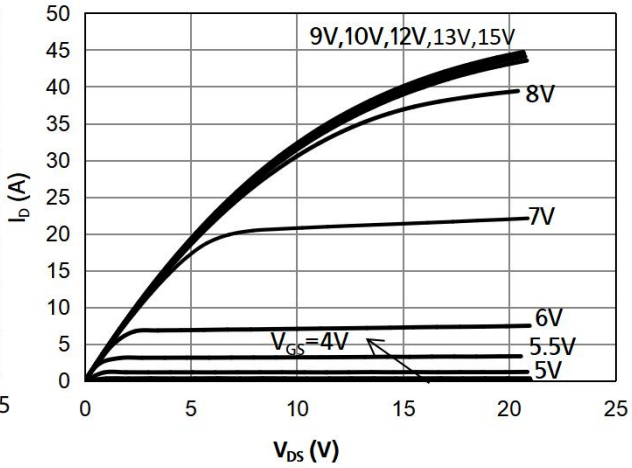


Fig 3: Transfer Characteristics

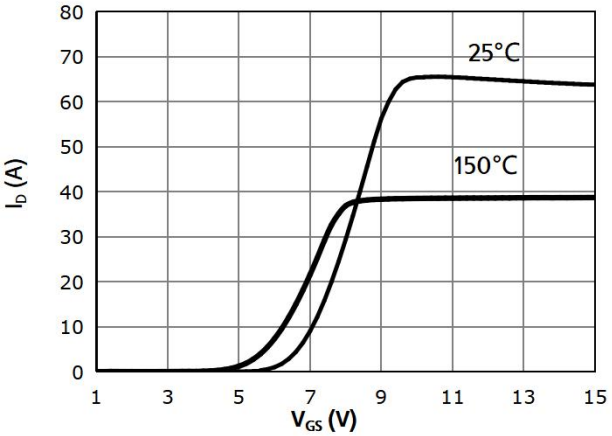


Fig 4: V_{TH} vs. T_j Temperature Characteristics

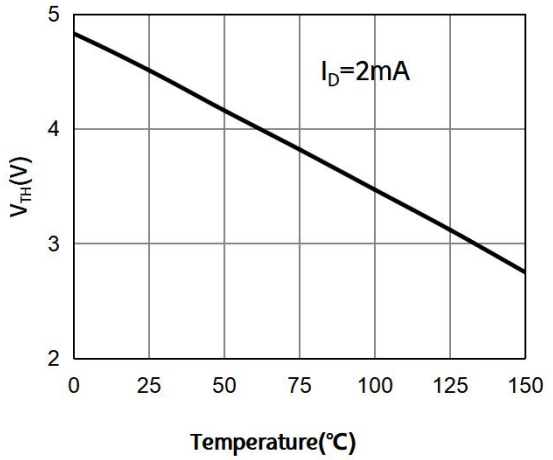


Fig 5: $R_{DS(on)}$ vs. I_{DS} Characteristics(T_j=25℃)

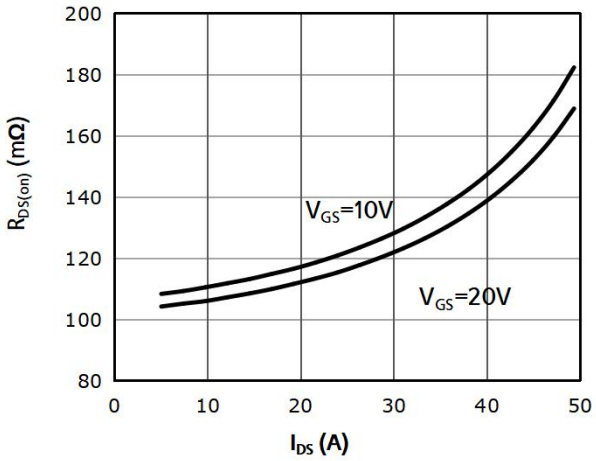


Fig 6: $R_{DS(on)}$ vs. Temperature

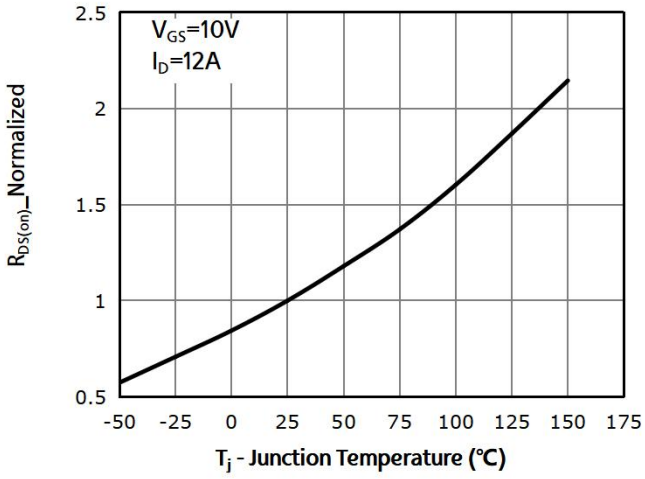


Fig 7: BV_{DSS} vs. Temperature

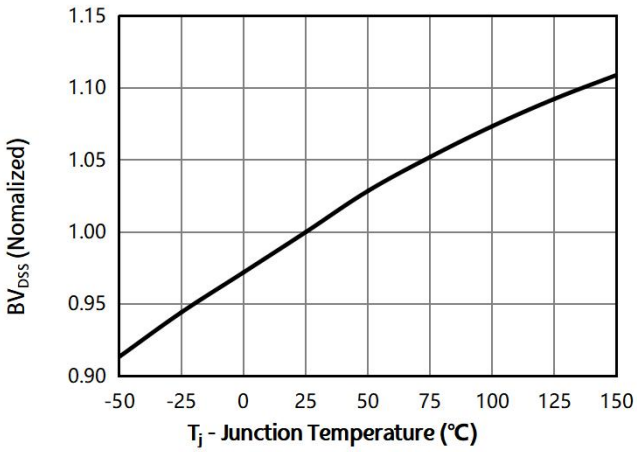


Fig 8: $R_{DS(on)}$ vs. Gate Voltage

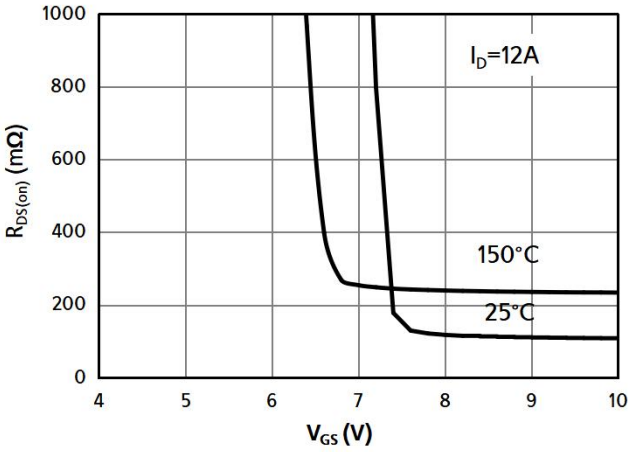


Fig 9: Body-diode Forward Characteristics

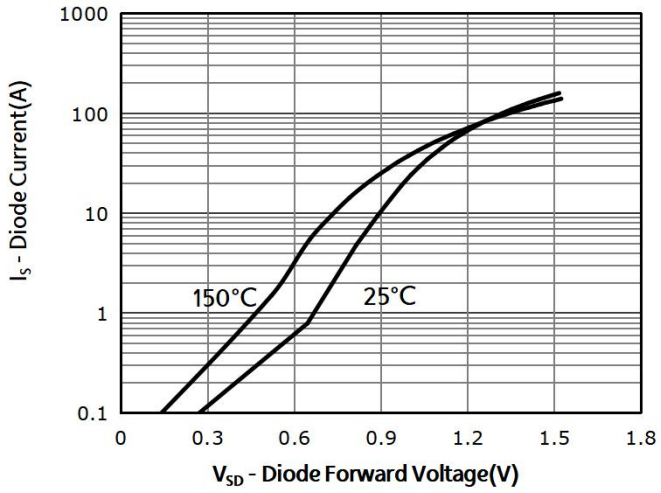


Fig 10: Gate Charge Characteristics

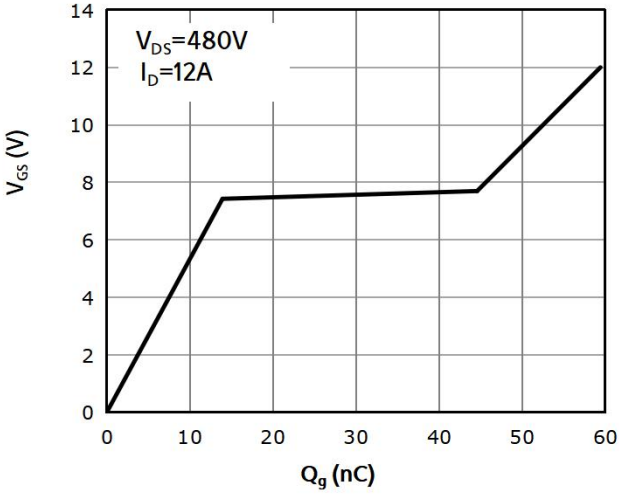


Fig 11: Capacitance Characteristics

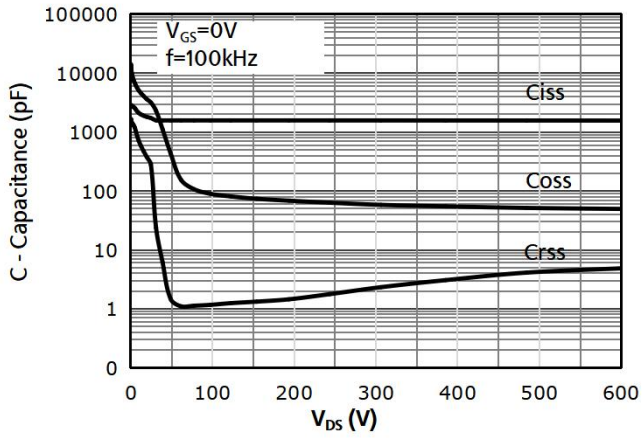


Fig 12: Safe Operating Area

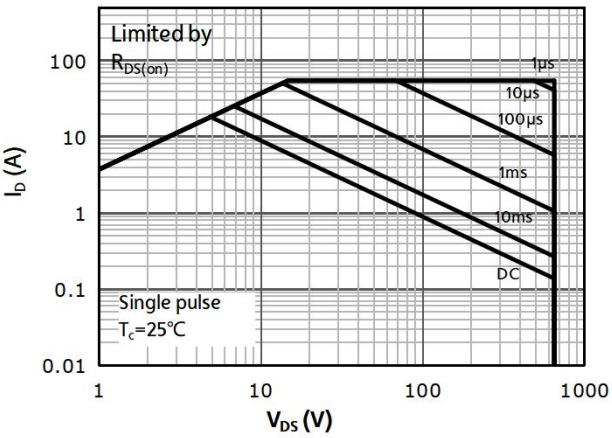
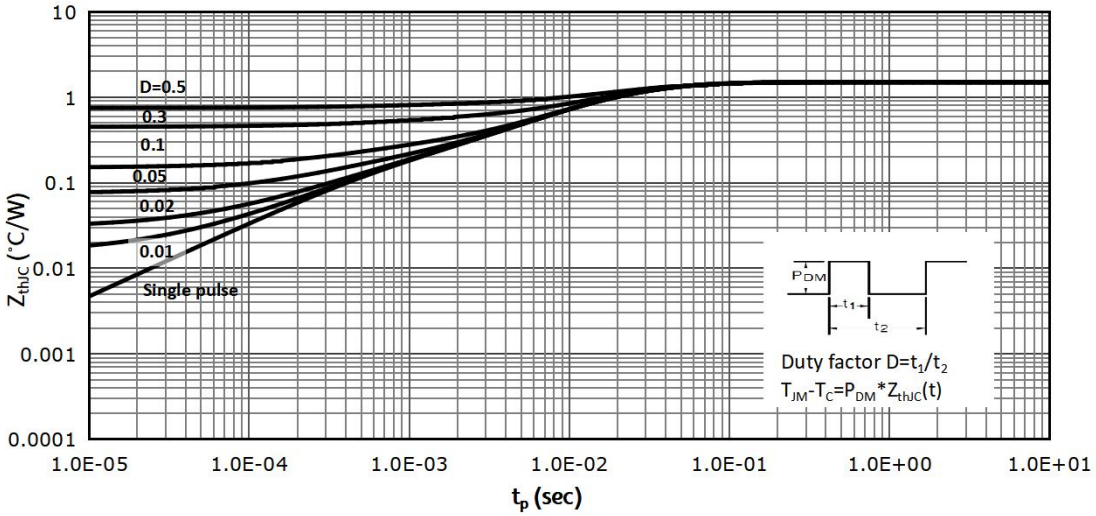
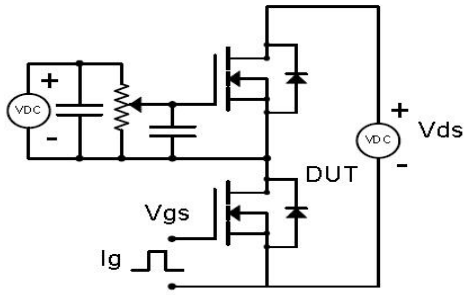


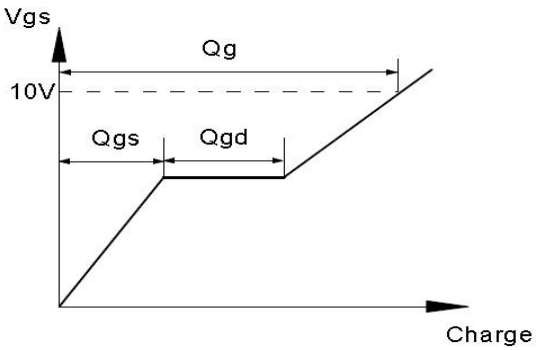
Fig 13: Max. Transient Thermal Impedance



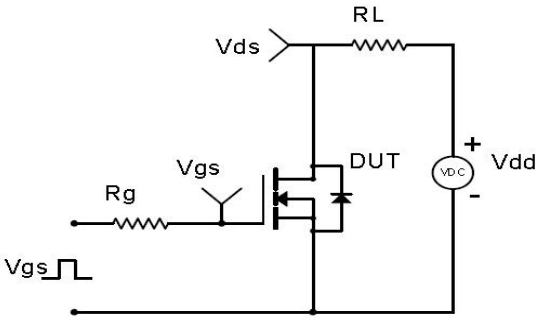
Test Circuit & Waveform

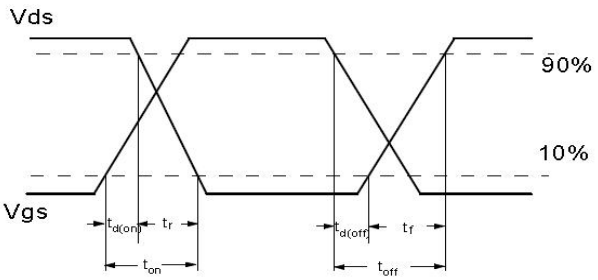
Gate Charge Test Circuit & Waveform



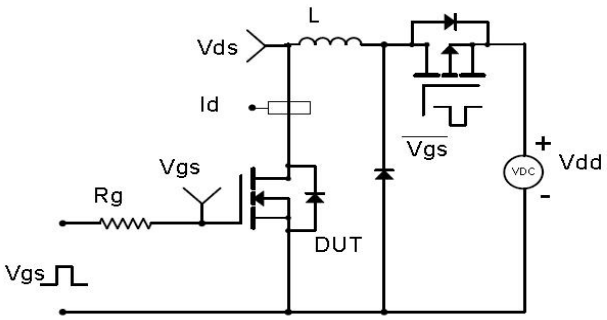


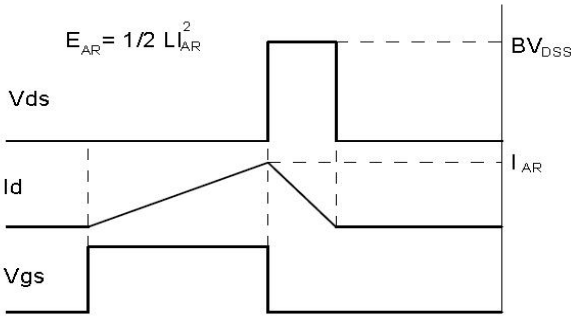
Resistive Switching Test Circuit & Waveforms



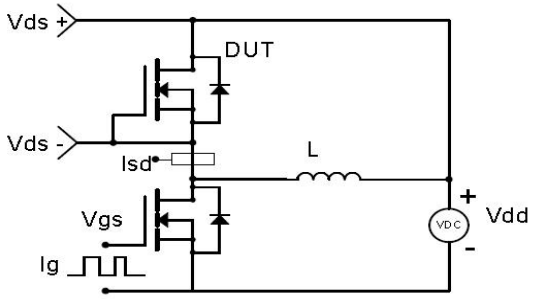


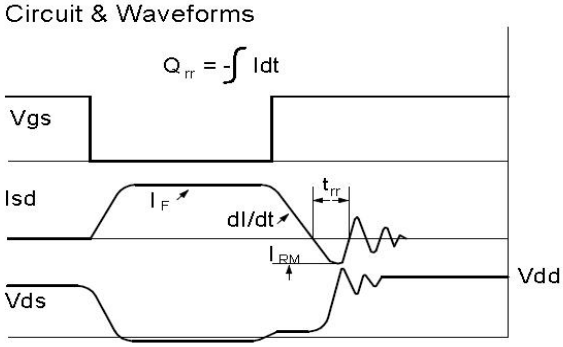
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



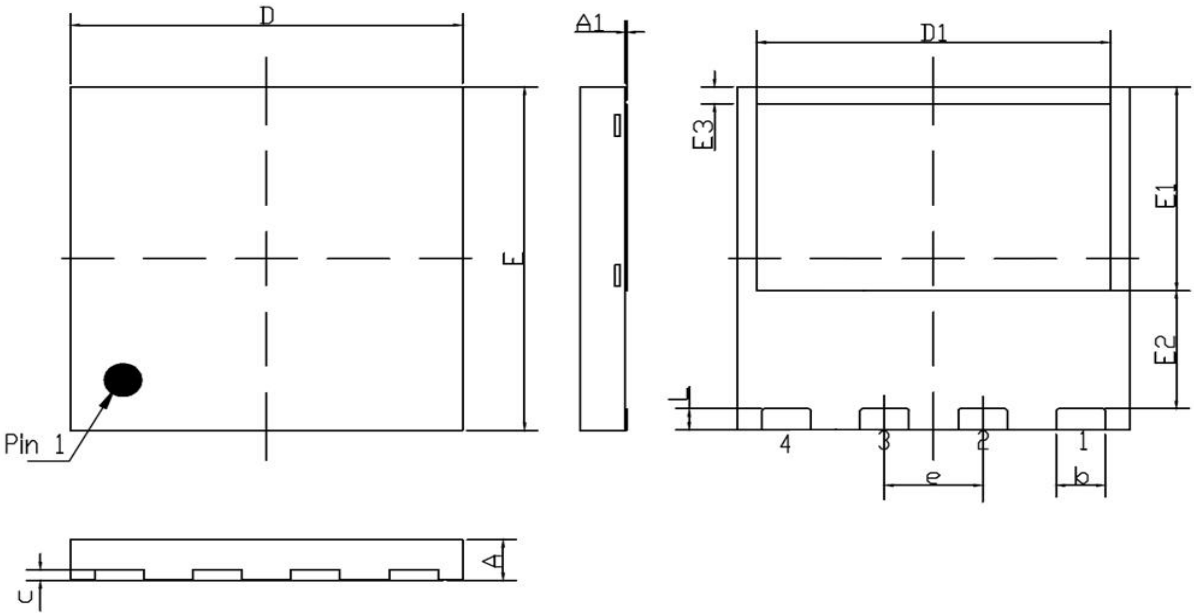


Diode Recovery Test Circuit & Waveforms





Package Outline: DFN8*8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.75	1.10	0.030	0.043
A1	0.00	0.05	0.000	0.002
b	0.90	1.10	0.035	0.043
c	0.10	0.30	0.004	0.012
D	7.90	8.10	0.311	0.319
D1	7.10	7.30	0.280	0.287
E	7.90	8.10	0.311	0.319
E1	4.65	4.85	0.183	0.191
E2	2.65	2.85	0.104	0.112
E3	0.30	0.50	0.012	0.020
e	2.00 BSC		0.079 BSC	
L	0.40	0.60	0.016	0.024

Marking



NOTE:
NXBBAAAA

N	—WB code (Usually omitted)
X	—Assembly location code
BB	—Fab code
AAAA	—Lot code

Revision History

Revison	Major changes
1.0	First version
1.1	Update Parameter
2.0	Update Datasheet Template

Disclaimer

Unless otherwise specified in the datasheet, the product is designed and qulified as a standard commercial product and is not intended for use in applications that require extraordinary levels of quality and reliability, such as automotive, aviation/aerospace and life-support devices or systems.
Any and all semicondutor products have certain probability to fail or malfunction, which may result in personal injury, death or property damage. Customer are solely responsible for providing adequate safe measures when design their systems.
CRM(CQ) reserves the right to improve product design, function and reliability without notice.