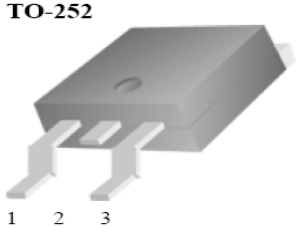
CS6R60 A4RDP-G

General Description：

CS6R60 A4RDP-G, the silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-252, which accords with the RoHS standard.

V_{DSS}	600	V
I_D	6	A
$P_D(T_C=25℃)$	79	W
$R_{DS(ON)Typ}$	1.6	Ω

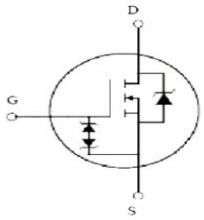
TO-252



1 2 3

1.Gate 2.Drain 3.Source

Inner Equivalent Principium Chart



Features：

- **Fast Switching**
- **Low ON Resistance(Rdson≤2.0Ω)**
- **Low Gate Charge (Typical Data: 20nC)**
- **Low Reverse transfer capacitances(Typical:1.5pF)**
- **100% Single Pulse avalanche energy Test**
- **Halogen Free**

Applications：

Power switch circuit of motor driver.

Absolute（T_J= 25℃ unless otherwise specified）：

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	600	V
I_D	Continuous Drain Current T_C = 25 °C	6	A
	Continuous Drain Current T_C = 100 °C	4.0	A
I_{DM} [a1]	Pulsed Drain Current T_C = 25 °C	24	A
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS} [a2]	Single Pulse Avalanche Energy	240	mJ
dv/dt [a3]	Peak Diode Recovery dv/dt	5.0	V/ns
P_D	Power Dissipation T_C = 25 °C	79	W
	Derating Factor above 25°C	0.60	W/℃
T_J， T_{stg}	Operating Junction and Storage Temperature Range	150，–55 to 150	℃

Electrical Characteristics（T_J= 25℃ unless otherwise specified）:

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	600	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Bvdss Temperature Coefficient	ID=250uA,Reference25℃	--	0.6	--	V/℃
I_{DSS}	Drain to Source Leakage Current	V_{DS} =600V, V_{GS}= 0V, T_J = 25℃	--	--	10	μA
		V_{DS} =480V, V_{GS}= 0V, T_J = 125℃	--	--	250	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS} =+20V	--	--	10	μA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS} =-20V	--	--	-10	μA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}=10V,I_D=3.0A	--	1.6	2.0	Ω
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	3.5	--	4.5	V
Pulse width tp≤300μs, δ ≤2%						

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g_{fs}	Forward Transconductance	V_{DS}=20V, I_D =3A	--	3.5	--	S
R_g	Gate resistance	f = 1.0MHz	--	4.3	--	Ω
C_{iss}	Input Capacitance	V_{GS} = 0V V_{DS} = 25V f = 1.0MHz	--	864	--	pF
C_{oss}	Output Capacitance		--	64	--	
C_{rss}	Reverse Transfer Capacitance		--	1.5	--	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	I_D =6A V_{DD} =300V V_{GS} = 10V R_G =10Ω	--	17.9	--	ns
tr	Rise Time		--	12.2	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	25.94	--	
t_f	Fall Time		--	13.74	--	
Q_g	Total Gate Charge	I_D =6A V_{DD} =480V V_{GS} = 10V	--	20	--	nC
Q_{gs}	Gate to Source Charge		--	5.7	--	
Q_{gd}	Gate to Drain (“Miller”)Charge		--	9.3	--	
Vp	Platform Voltage			6.39		V

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)		--	--	6	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	24	A
V_{SD}	Diode Forward Voltage	I_S=6.0A,V_{GS}=0V	--	--	1.5	V
trr	Reverse Recovery Time	I_S=6.0A,T_j = 25℃ dI$_F$/dt=100A/us, V_{GS}=0V	--	60	120	ns
Qrr	Reverse Recovery Charge		--	98	--	nC
I_{RRM}	Reverse Recovery Current		--	3.3	--	A
Pulse width tp≤300μs, δ ≤2%						

Symbol	Parameter	Max	Units
$R_{\theta JC}$	Junction-to-Case	1.58	℃/W
$R_{\theta JA}$	Junction-to-Ambient	100	℃/W

Gate-source Zener diode						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{GSO}	Gate-source breakdown voltage	I_{GS}= ±1mA(Open Drain)	30			V
The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.						

[a1]: Repetitive rating; pulse width limited by maximum junction temperature
[a2]: L=10mH, I_D=6.9A, Start T_J=25℃
[a3]: I_{SD} =6A,di/dt ≤100A/us,V_{DD}≤$BV_{DS,}$ Start T_J=25℃
[a4]: Recommend soldering temperature defined by IPC/JEDEC J-STD 020

Characteristics Curve:

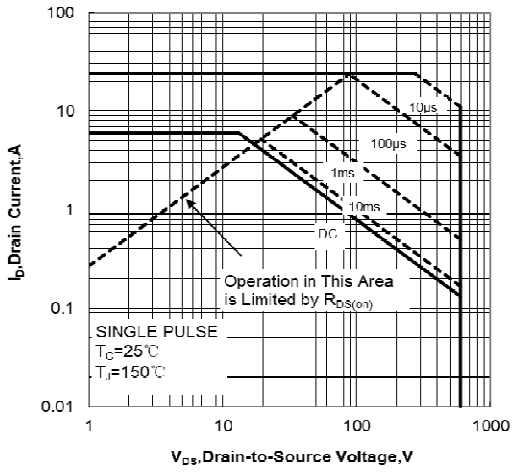


Figure.1 Maximum Forward Bias Safe Operating Area

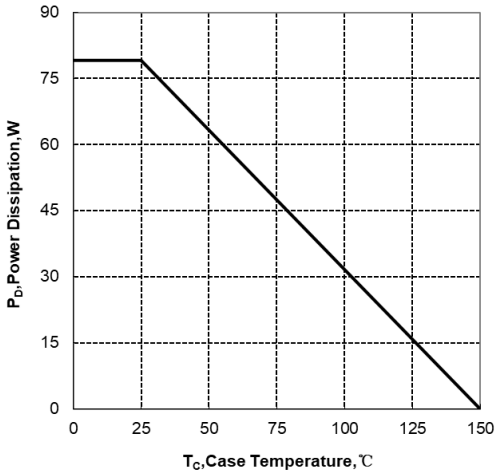


Figure.2 Maximum Power Dissipation vs Case Temperature

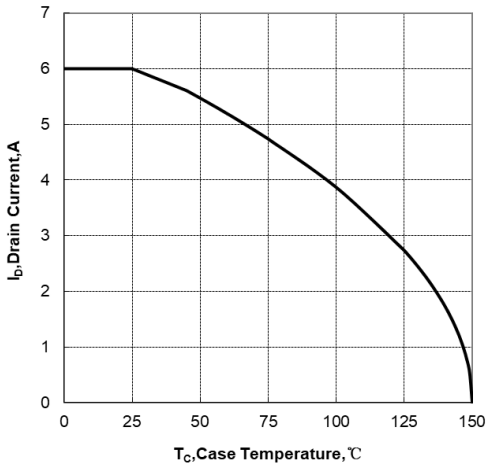


Figure.3 Maximum Continuous Drain Current vs Case Temperature

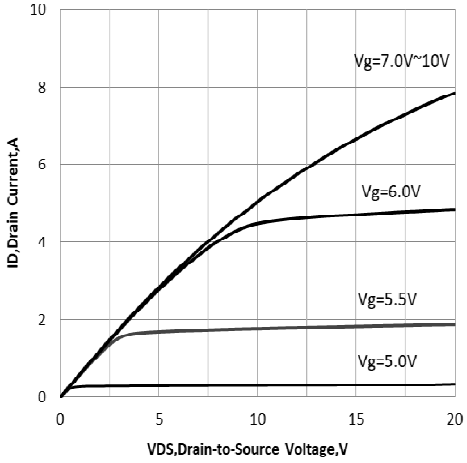


Figure.4 Typical Output Characteristics

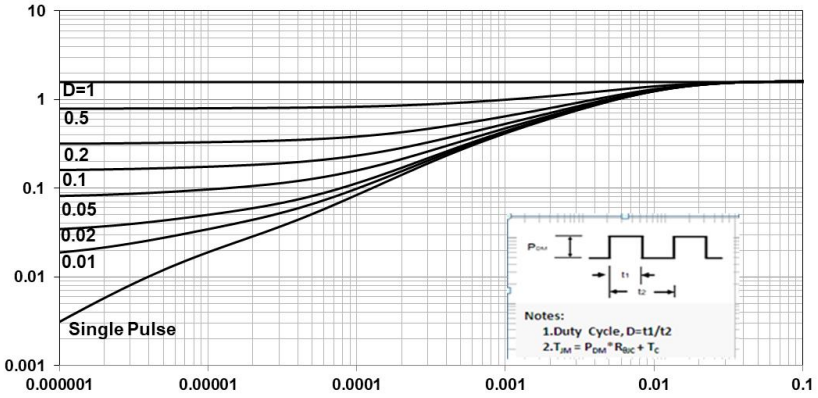


Figure.5 Maximum Effective Thermal Impedance , Junction to Case

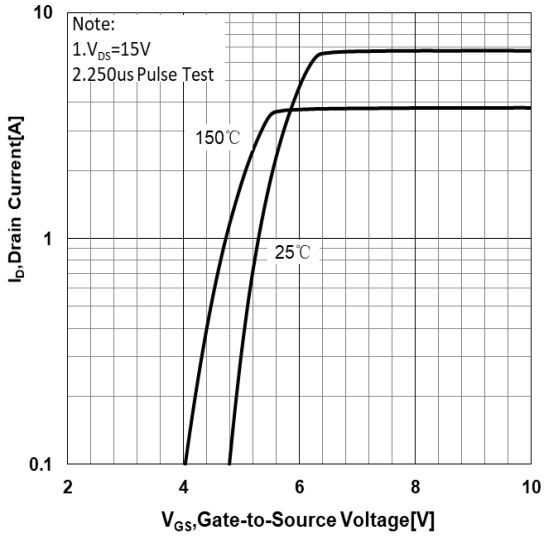


Figure.6 Typical Transfer Characteristics

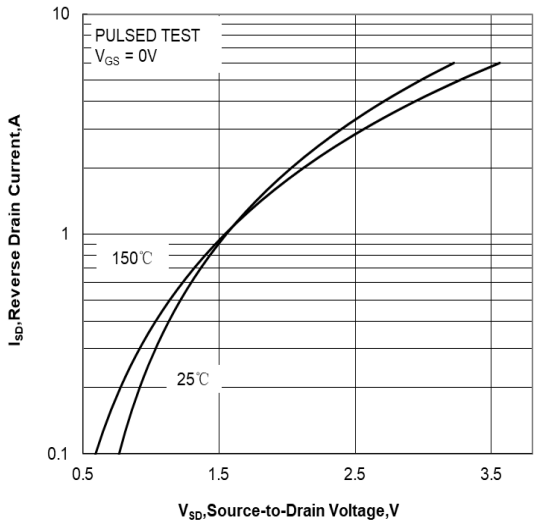


Figure.7 Typical Body Diode Transfer Characteristics

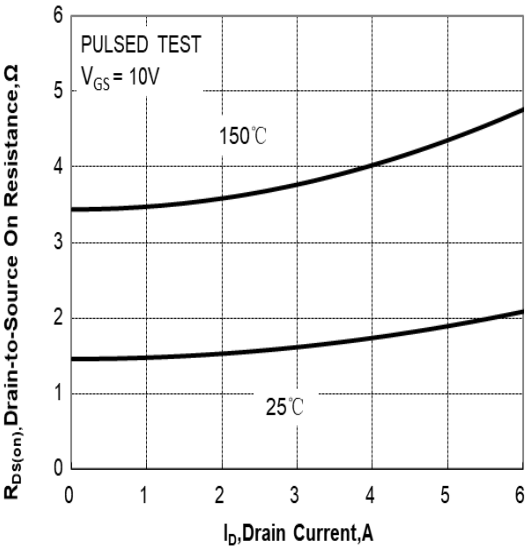


Figure.8 Typical Drain to Source ON Resistance vs Drain Current

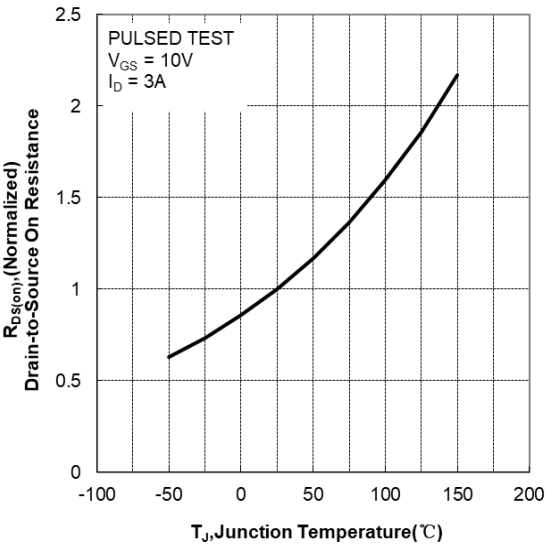


Figure.9 Typical Drian to Source on Resistance vs Junction Temperature

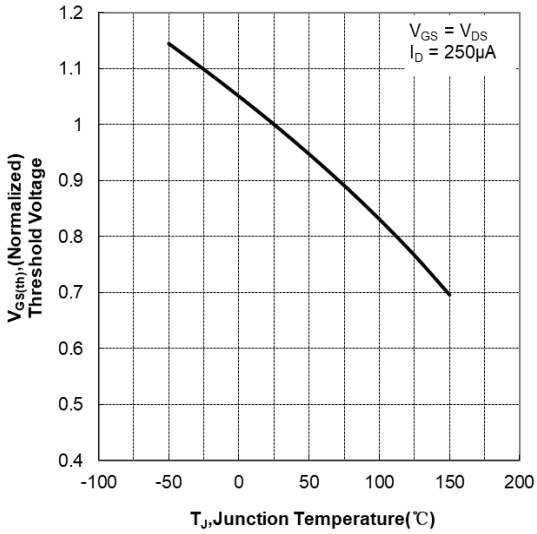


Figure.10 Typical Theshold Voltage vs Junction Temperatu

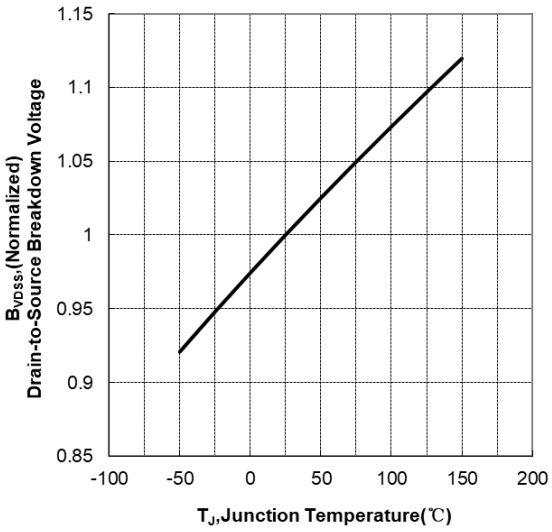


Figure 11 Typical Breakdown Voltage vs Junction Temperature

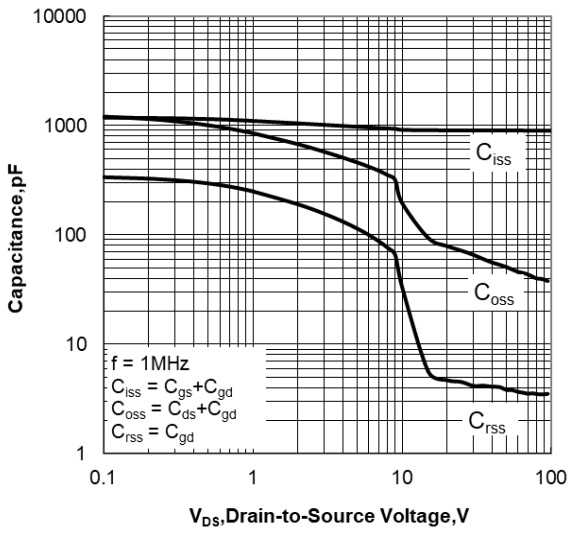


Figure.12 Typical Capacitance vs Drain to Source Voltage

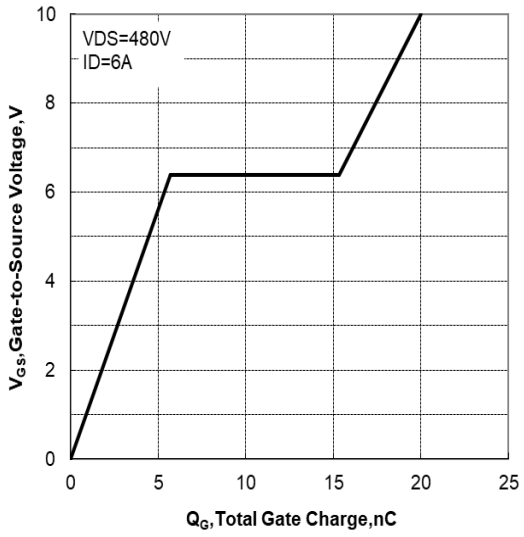


Figure.13 Typical Gate Charge vs Gate to Source Voltage

Test Circuit and Waveform

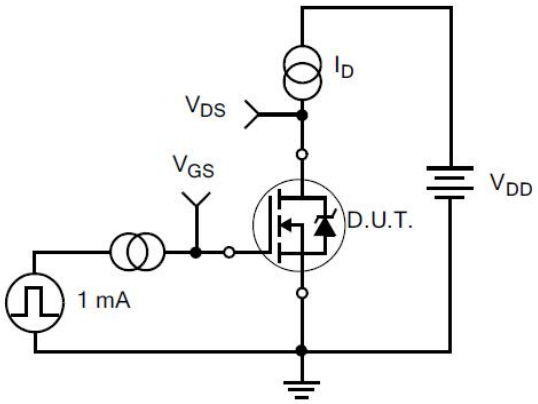


Figure 14. Gate Charge Test Circuit

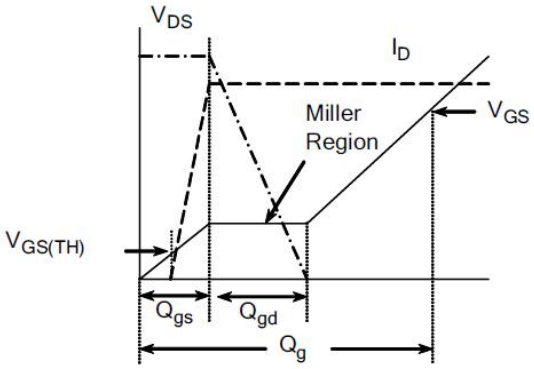


Figure 15. Gate Charge Waveforms

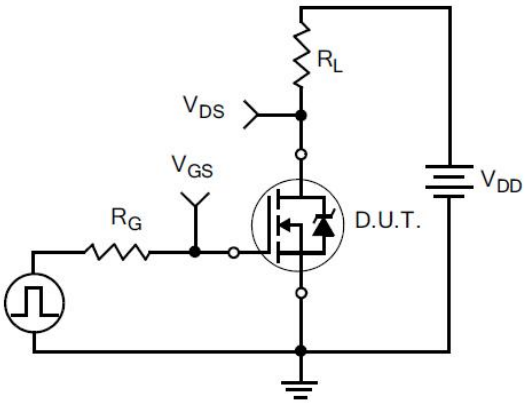


Figure 16. Resistive Switching Test Circuit

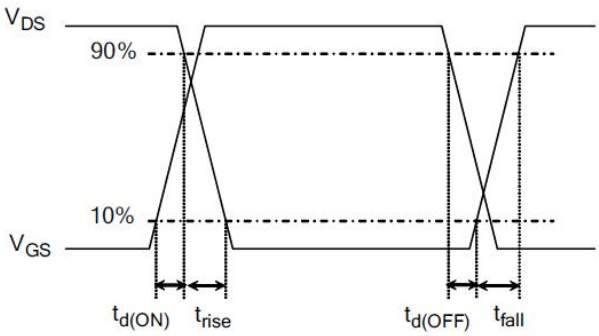


Figure 17. Resistive Switching Waveforms

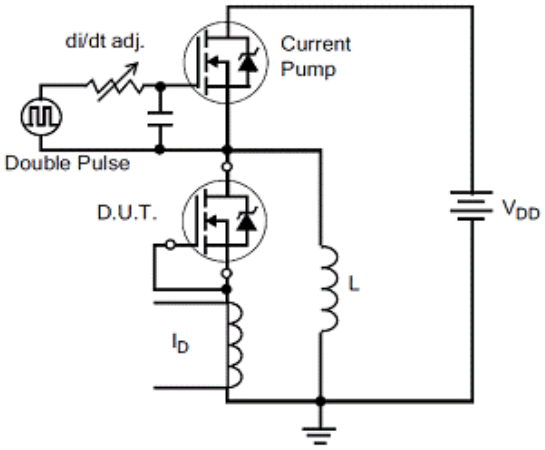


Figure 18. Diode Reverse Recovery Test Circuit

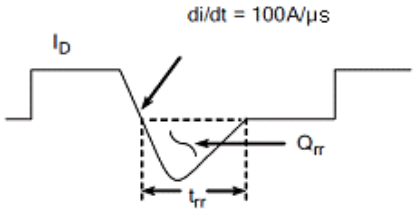


Figure 19. Diode Reverse Recovery Waveform

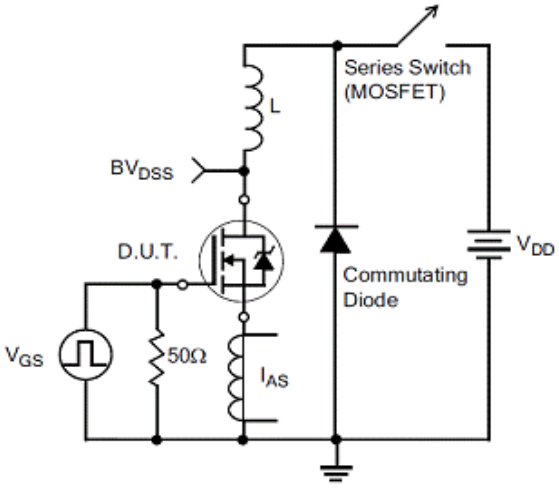


Figure20.Unclamped Inductive Switching Test Circuit

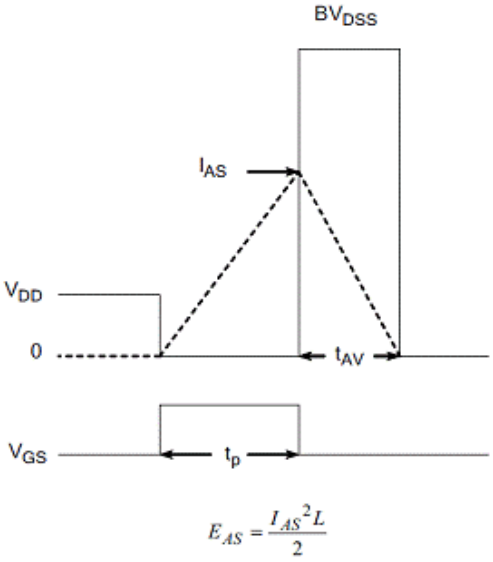
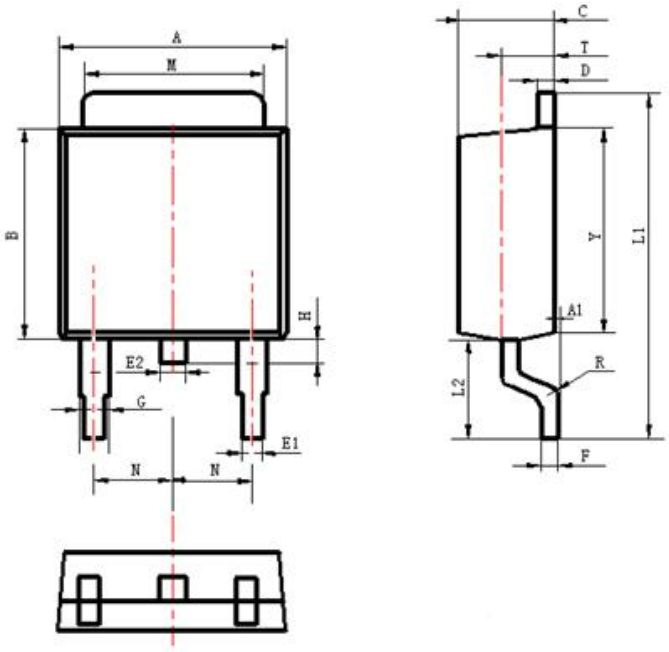


Figure21.Unclamped Inductive Switching Waveform

Package Information：



Items	Values(mm)	
	MIN	MAX
A	6.30	6.90
A1	0	0.16
B	5.70	6.30
C	2.10	2.50
D	0.30	0.70
E1	0.60	0.90
E2	0.70	1.00
F	0.30	0.60
G	0.70	1.20
L1	9.60	10.50
L2	2.70	3.10
H	0.40	1.00
M	5.10	5.50
N	2.09	2.49
R	0.3	
T	1.40	1.60
Y	5.10	6.30

TO-252 Package

The name and content of poisonous and harmful material in products

	Hazardous Substance									
	Pb	Hg	Cd	Cr(VI)	PBB	PBDE	DIBP	DEHP	DBP	BBP
Limit	≤0.1%	≤0.1%	≤ 0.01%	≤0.1%	≤0.1%	≤0.1%	≤0.1%	≤0.1%	≤0.1%	≤0.1%
Lead Frame	○	○	○	○	○	○	○	○	○	○
Molding	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
Wire Bonding	○	○	○	○	○	○	○	○	○	○
Solder	×	○	○	○	○	○	○	○	○	○
Note	○: Means the hazardous material is under the criterion of 2011/65/EU. ×: Means the hazardous material exceeds the criterion of 2011/65/EU. The plumbum element of solder exist in products presently, but within the allowed range of Eurogroup's RoHS.									

Warnings

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. It is suggested to be used under 80 percent of the maximum ratings of the device.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. VDMOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. This publication is made by Huajing Microelectronics and subject to regular change without notice.

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