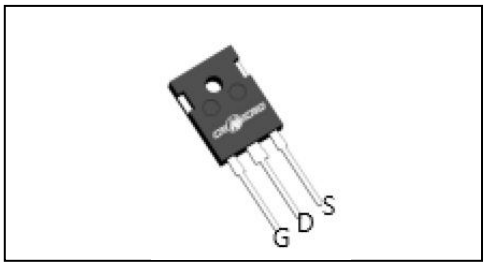
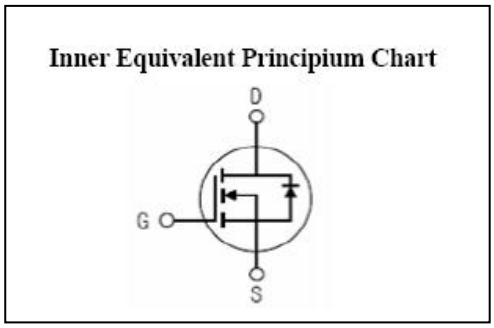
General Description：

CS40N50AKR-G,the silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-247, which accords with the RoHS standard.

V_{DSS}	500	V
I_D	40	A
P_D(T_C=25℃)	250	W
$R_{DS(ON)Typ}$	85	mΩ





Features：

- Fast Switching
- Low ON Resistance(Rdson≤100mΩ)
- Low Reverse transfer capacitances(Typical:4.3pF)
- 100% Single Pulse avalanche energy Test
- Halogen Free
- Qualified according to JEDEC criteria

Applications：

Power switch circuit of electron ballast and adaptor.

Package Parameters

Type	Marking	Package	Packing
CS40N50AKR-G	CS40N50AKR-G	TO-247	Tube

Absolute（T_J= 25℃ unless otherwise specified）：

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	500	V
I_D	Continuous Drain Current T_C = 25 °C	40	A
	Continuous Drain Current T_C = 100 °C	25	A
I_{DM} [a1]	Pulsed Drain Current T_C = 25 °C	160	A
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS} [a2]	Single Pulse Avalanche Energy	3363	mJ
dv/dt [a3]	Peak Diode Recovery dv/dt	5.0	V/ns
P_D	Power Dissipation T_C = 25 °C	250	W
	Derating Factor above 25°C	2	W/℃
T_J，T_{stg}	Operating Junction and Storage Temperature Range	150，–55 to 150	℃

Electrical Characteristics（T_J= 25℃ unless otherwise specified）：

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	500	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Bvdss Temperature Coefficient	ID=250uA, Reference25℃	--	0.6	--	V/℃
I_{DSS}	Drain to Source Leakage Current	V_{DS} =500V, V_{GS}= 0V, T_J = 25℃	--	--	1	μA
		V_{DS} =400V, V_{GS}= 0V, T_J = 125℃	--	--	100	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS} =+30V	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS} =-30V	--	--	-100	nA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}=10V,I_D=20A	--	85	100	mΩ
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D = 250μA	2.5	--	4.5	V
Pulse width tp≤300μs,δ≤2%						

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g_{fs}	Forward Trans conductance	V_{DS}=15V, I_D =20A	--	36	--	S
Rg	Gate resistance	f = 1.0MHz	--	2.5	--	Ω
C_{iss}	Input Capacitance	V_{GS} = 0V V_{DS} = 25V f = 1.0MHz	--	8458	--	pF
C_{oss}	Output Capacitance		--	695	--	
C_{rss}	Reverse Transfer Capacitance		--	4.3	--	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	I_D =40A V_{DD} = 250V R_G =25Ω	--	146	--	ns
tr	Rise Time		--	180	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	330	--	
t_f	Fall Time		--	140	--	
Q_g	Total Gate Charge	I_D =40A V_{DD} =400V V_{GS} = 10V	--	137	--	nC
Q_{gs}	Gate to Source Charge		--	46	--	
Q_{gd}	Gate to Drain (“Miller”)Charge		--	40	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)	T_C = 25 °C	--	--	40	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	160	A
V_{SD}	Diode Forward Voltage	I_S=40A,V_{GS}=0V	--	--	1.5	V
trr	Reverse Recovery Time	I_S=40A,T_j= 25℃ dI$_F$/dt=100A/us, V_{GS}=0V	--	605	--	ns
Qrr	Reverse Recovery Charge		--	9380	--	nC
I_{RRM}	Reverse Recovery Current		--	31	--	A

Symbol	Parameter	Max.	Units
$R_{\theta JC}$	Junction-to-Case	0.5	℃/W
$R_{\theta JA}$	Junction-to-Ambient	40	℃/W

[a1]: Repetitive rating; pulse width limited by maximum junction temperature
[a2]: L=10mH, I_D=26A, Start T_J=25℃
[a3]: I_{SD} =40A,di/dt ≤100A/us,V_{DD}≤$BV_{DS,}$ Start T_J=25℃

Characteristics Curve:

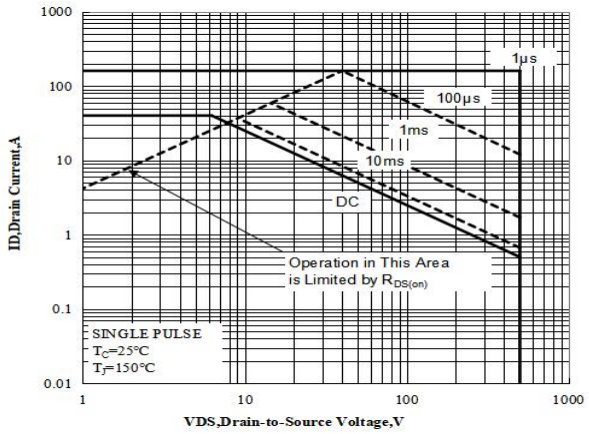


Figure 1 Maximum Forward Bias Safe Operating Area

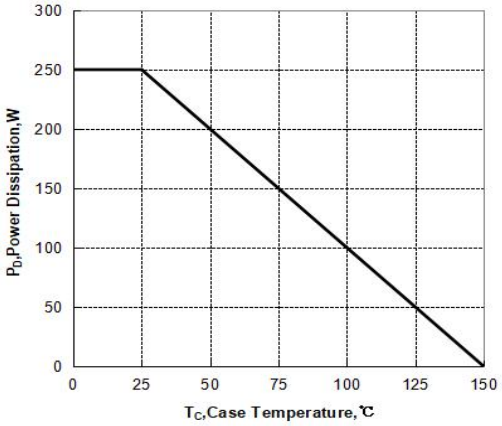


Figure 2 Maximum Power dissipation vs Case Temperature

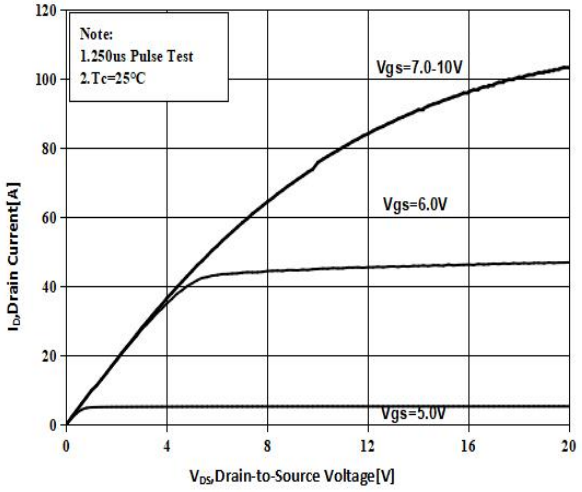


Figure 3 Maximum Continuous Drain Current vs Case Temperature

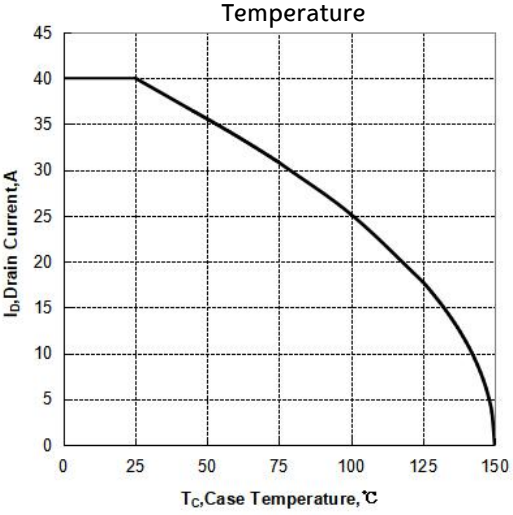


Figure 4 Typical Output Characteristics

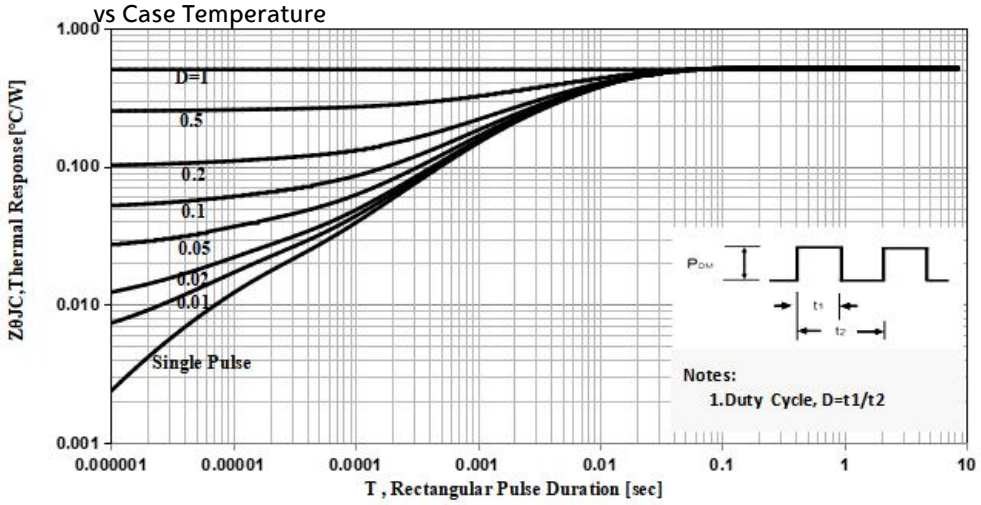


Figure 5 Maximum Effective Thermal Impedance

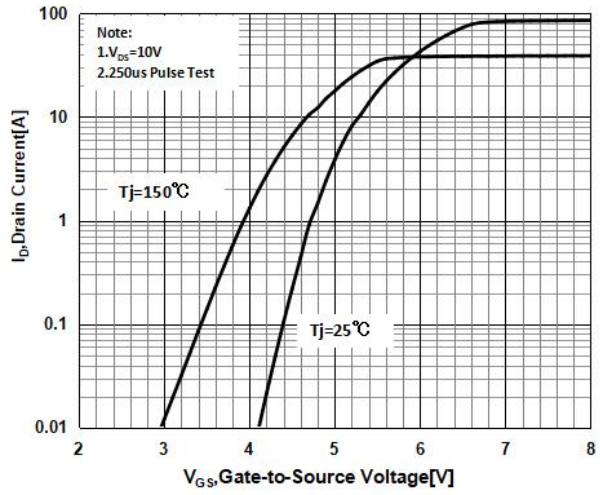


Figure 6 Typical Transfer Characteristics

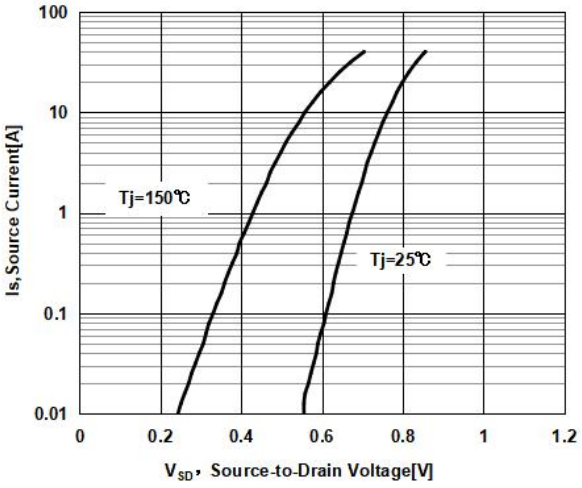


Figure 7 Typical Body Diode Transfer Characteristics

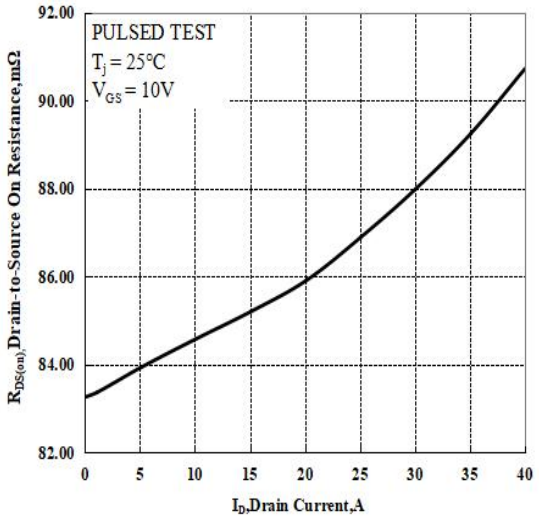


Figure 8 Typical Drain to Source ON Resistance vs Drain Current

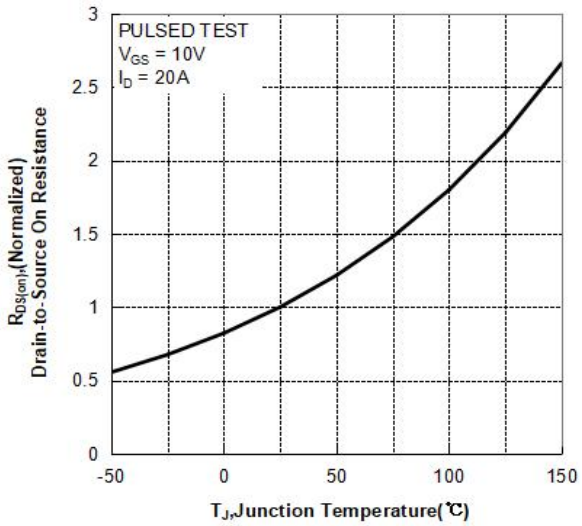


Figure 9 Typical Drian to Source on Resistance vs Junction Temperature

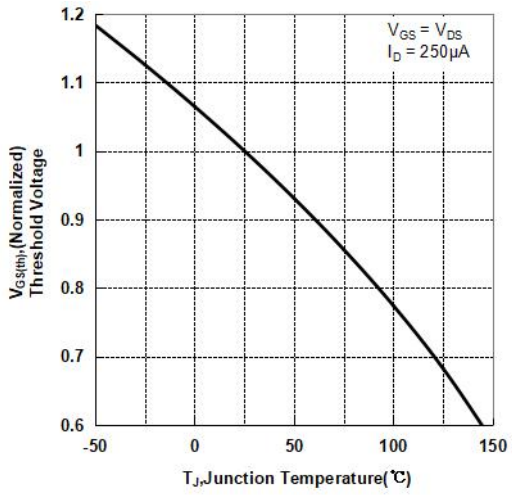


Figure 10 Typical Theshold Voltage vs Junction Temperature

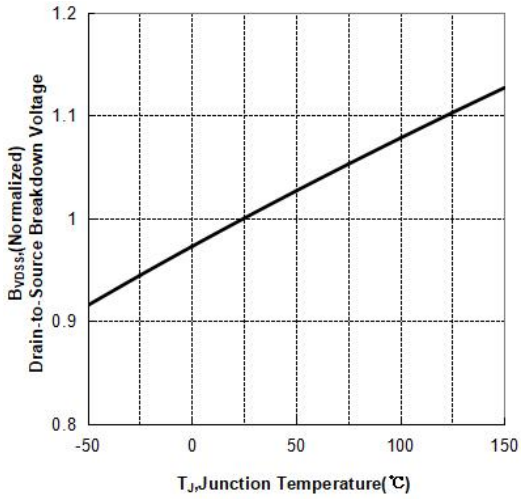


Figure11 Typical Breakdown Voltage vs Junction Temperature

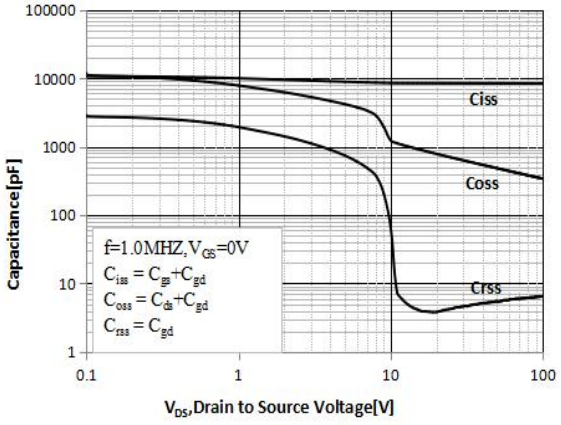


Figure 12 Typical Capacitance vs Drain to Source Voltage

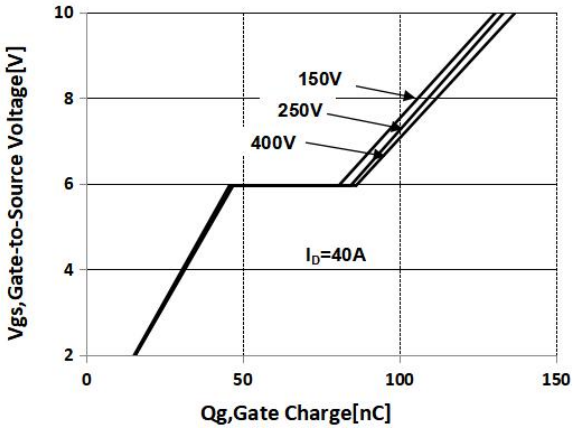
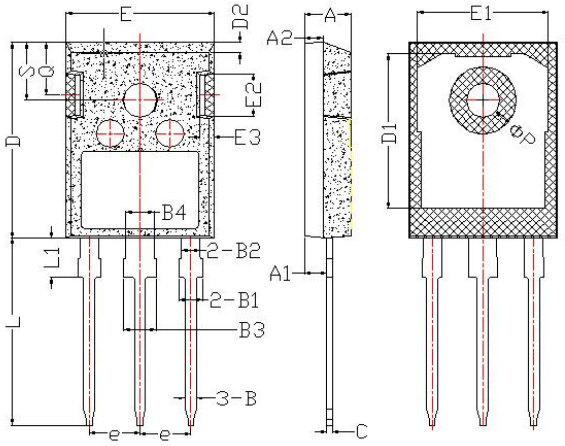


Figure 13 Typical Gate Charge vs Gate to Source Voltage

Package Information：



Items	Values(mm)	
	MIN	MAX
A	4.6	5.2
A1	2,2	2.6
A2	1.85	2.17
B	0.9	1.4
B1	1.75	2.35
B2	1.75	2.15
B3	2.8	3.35
B4	2.8	3.15
C	0.5	0.7
D	20.60	21.30
D1	16	18
E	15.5	16.10
E1	13	14.7
E2	3.80	5.3
E3	0.8	2.60
e	5.2	5.7
L	19	20.5
L1	3.9	4.6
ΦP	3.3	3.70
ΦP1	7.0	7.4
Q	5.2	6.00
S	5.8	6.6

TO-247 Package

Warnings

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. It is suggested to be used under 80 percent of the maximum ratings of the device.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. VDMOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. This publication is made by Huajing Microelectronics and subject to regular change without notice.

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Revison History		
Revision	Date	Major changes
1.0	2026/1/27	Initial release