HK24C128/ HK24C256

I²C-Compatible (2-wire) Serial EEPROM

128Kbit(16,384X8) /256Kbit(32,768X8)

Ultra Low Power EEPROM Datasheet

FEATURES

- Low power consumption:
  - Standby current : 10nA@Typical, Max<1000nA
  - Read current: 500uA@Typical, Max<1000uA
  - Write current: 500uA@Typical, Max<1000uA
- HK24C128/256: V CC = 1.8V to 5.5V
- 64 bytes page write mode.
- Partial page write operation allowed.
- Internally organized: 16,384x 8 (128K)/32,768x8(256K).
- Standard 2-wire bi-directional serial interface.
- Schmitt trigger, filtered inputs for noise protection.
- Self-timed Write Cycle (5ms maximum).
- 1 MHz (5V), 400 kHz (1.8V, 2.5V, 2.7V) Compatibility.
- Automatic erase before write operation.
- Write protect pin for hardware data protection.
- High reliability: typically 1, 000,000 cycles endurance.
- 100 years data retention.
- Industrial temperature range (-40℃ to 85℃).
- Standard 8-lead DIP/SOP/MSOP/TSSOP/DFN and 5-lead SOT-23/TSOT-23/CSP Pb-free packages.

DESCRIPTION

The HK24C128/256 is 131,072/262,144 bits of serial Electrical Erasable and Programmable Read Only Memory, commonly known as EEPROM. They are organized as 16,384/32,768 words of 8 bits (1 byte) each. These devices are available in standard 8-lead DIP, 8-lead SOP, 8-lead TSSOP, 8-lead DFN, 8-lead MSOP, and 5-lead SOT-23/TSOT-23 packages. A standard 2-wire serial interface is used to address all read and write functions. Our extended VCC range (1.8V to 5.5V) devices enables wide spectrum of applications.

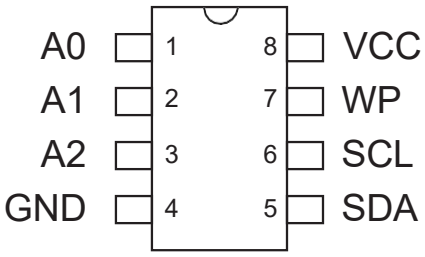
1. PIN CONFIGURATION

Table-A Pin Configuration

Pin Name	Pin Function
A2, A1, A0	Device Address Inputs
SDA	Serial Data Input / Open Drain Output
SCL	Serial Clock Input
WP	Write Protect
NC	No-Connect

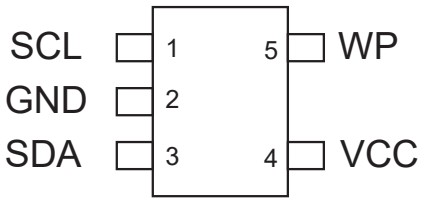
All these packaging types come in conventional or Pb-free certified.

HK24C128/
HK24C256



8L DIP
8L SOP
8L MSOP
8L TSSOP
8L DFT

HK24C128/
HK24C256



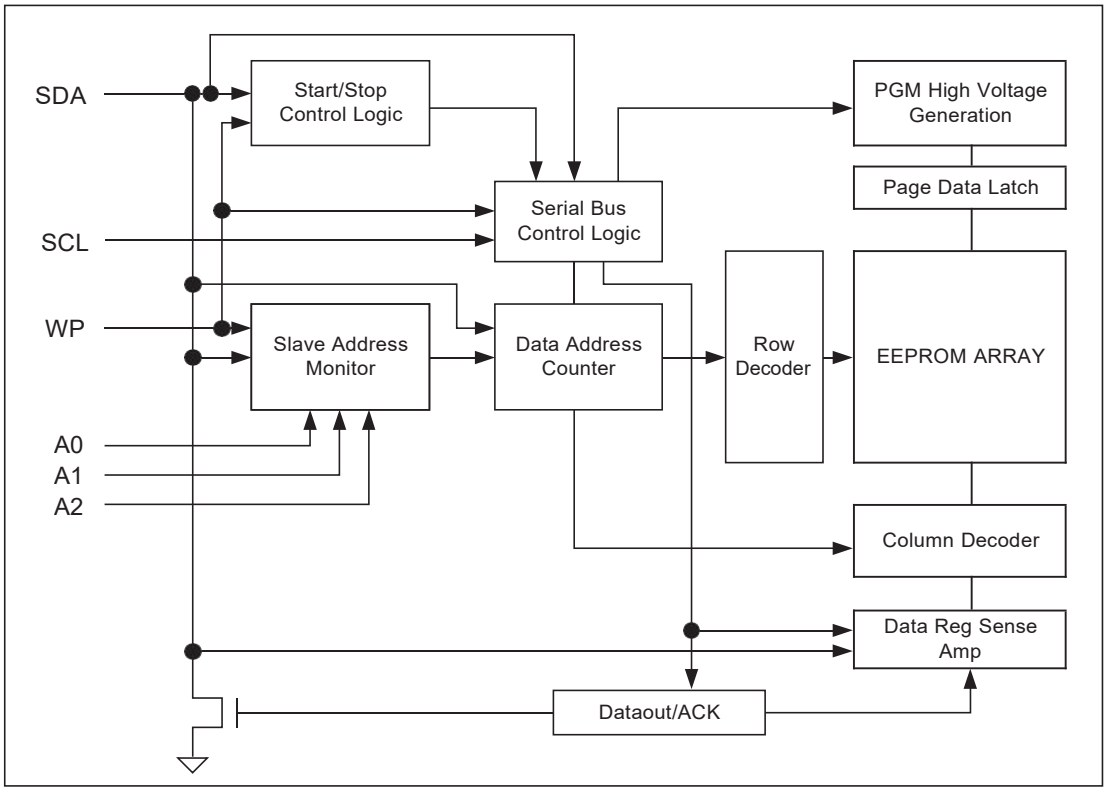
5L SOT-23
5LTSOT-23

2. ABSOLUTE MAXIMUM RATINGS

Industrial operating temperature:	-40℃ to 85℃
Storage temperature:	-50℃ to 125℃
Input voltage on any pin relative to ground:	-0.3V to VCC + 0.3V
Maximum voltage:	8V
ESD protection on all pins:	>2000V

** Stresses exceed those listed under "Absolute Maximum Rating" may cause permanent damage to the device. Functional operation of the device at conditions beyond those listed in the specification is not guaranteed. Prolonged exposure to extreme conditions may affect device reliability or functionality*.

1. BLOCK DIAGRAM



2. PIN DESCRIPTIONS

(A) SERIAL CLOCK (SCL)

The rising edge of this SCL input is to latch data into the EEPROM device while the falling edge of this clock is to clock data out of the EEPROM device.

(B) DEVICE / CHIP SELECT ADDRESSES (A2, A1, A0)

These are the chip select input signals for the serial EEPROM devices. Typically, these signals are hardwired to either VIH or VIL. If left unconnected, they are internally recognized as VIL.

(C) SERIAL DATA LINE (SDA)

SDA data line is a bi-directional signal for the serial devices. It is an open drain output signal and can be wired-OR with other open-drain output devices.

(D) WRITE PROTECT (WP)

The HK24C128/256 devices have a WP pin to protect the whole EEPROM array from programming. Programming operations are allowed if WP pin is left un-connected or input to VIL. Conversely all programming functions are disabled if WP pin is connected to VIH or VCC. Read operations is not affected by the WP pin’s input level.

3. MEMORY ORGANIZATION

The HK24C128/256 devices have 256/512 pages respectively. Since each page has 64 bytes,
random word addressing to HK24C128/256 will require 14/15 bits data word addresses respectively.

4. DEVICE OPERATION

(A) SERIAL CLOCK AND DATA TRANSITIONS

The SDA pin is typically pulled to high by an external resistor. Data is allowed to change only when Serial clock SCL is at VIL. Any SDA signal transition may interpret as either a START or STOP condition as described below.

(B) START CONDITION

With SCL VIH, a SDA transition from high to low is interpreted as a START condition. All valid commands must begin with a START condition(Figure 1).

(C) STOP CONDITION

With SCL VIH, a SDA transition from low to high is interpreted as a STOP condition. All valid read or write commands end with a STOP condition. The device goes into the STANDBY mode if it is after a read command. A STOP condition after page or byte write command will trigger the chip into the STANDBY mode after the self-timed internal programming finish(Figure 1).

(D) ACKNOWLEDGE

The 2-wire protocol transmits address and data to and from the EEPROM in 8 bit words. The EEPROM acknowledges the data or address by outputting a "0" after receiving each word. The ACKNOWLEDGE signal occurs on the 9th serial clock after each word(Figure 2).

(E) STANDBY MODE

The EEPROM goes into low power STANDBY mode after a fresh power up, after receiving a STOP bit in read mode, or after completing a self-time internal programming operation.

Figure 1: Timing diagram for START and STOP condition

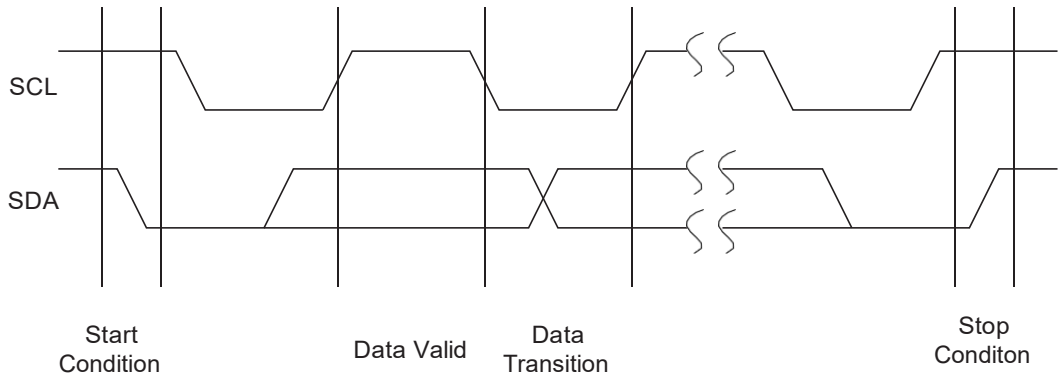
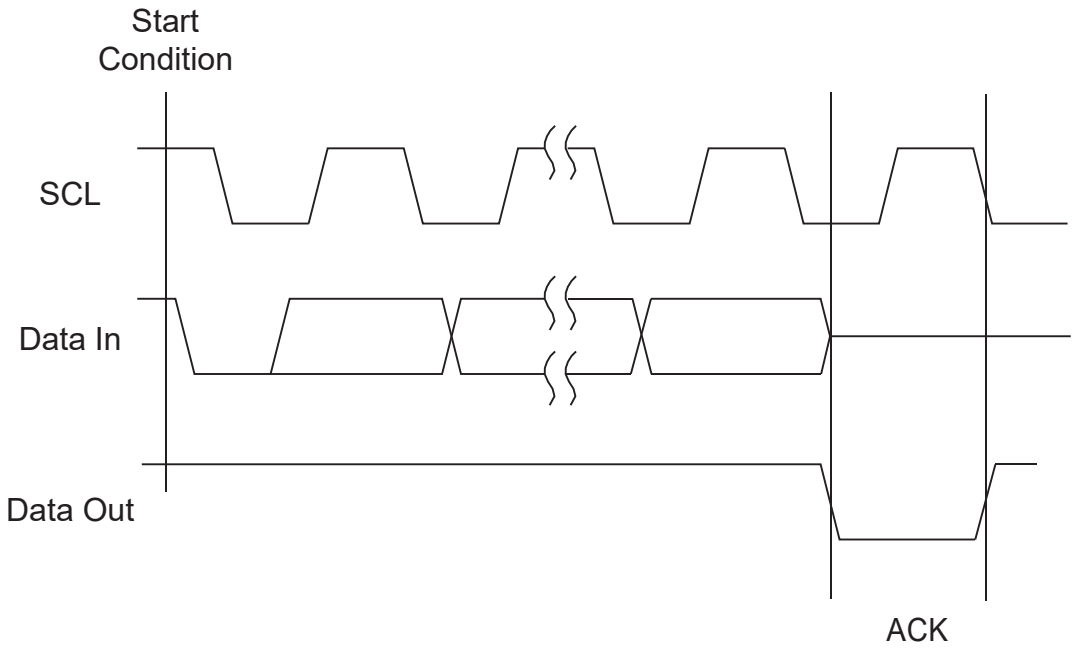


Figure2: Timing diagram for output ACKNOWLEDGE



5. DEVICE ADDRESSING

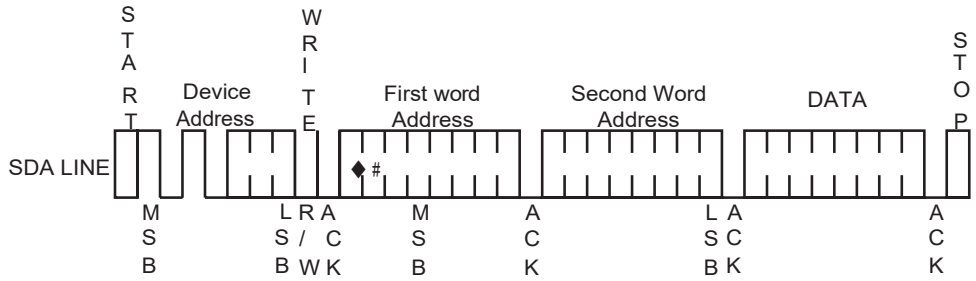
The 2-wire serial bus protocol mandates an 8 bits device address word after a START bit condition to invoke valid read or write command. The first four most significant bits of the device address must be 1010, which is common to all serial EEPROM devices. The next three bits are device address bits. These three device address bits (5th, 6th and 7th) are to match with the external chip select/address pin states. If a match is made, the EEPROM device outputs an ACKNOWLEDGE signal after the 8th read/write bit, otherwise the chip will go into STANDBY mode. However, matching may not be needed for some or all device address bits (5th, 6th and 7th) as noted below. The last or 8th bit is a read/write command bit. If the 8th bit is at VIH then the chip goes into read mode. If a “0” is detected, the device enters programming mode.

6. WRITE OPERATIONS

(A) BYTE WRITE

A write operation requires two 8-bit data word address following the device address word and ACKNOWLEDGE signal. Upon receipt of this address, the EEPROM will respond with a “0” and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will again output a “0”. The addressing device, such as a microcontroller, must terminate the write sequence with a STOP condition. At this time the EEPROM enters into an internally-timed write cycle state. All inputs are disabled during this write cycle and the EEPROM will not respond until the writing is completed (figure 3).

Figure 3: Byte Write



Notes:

1) *=Don't care bits
2) #=Don't care bits for HK24C128

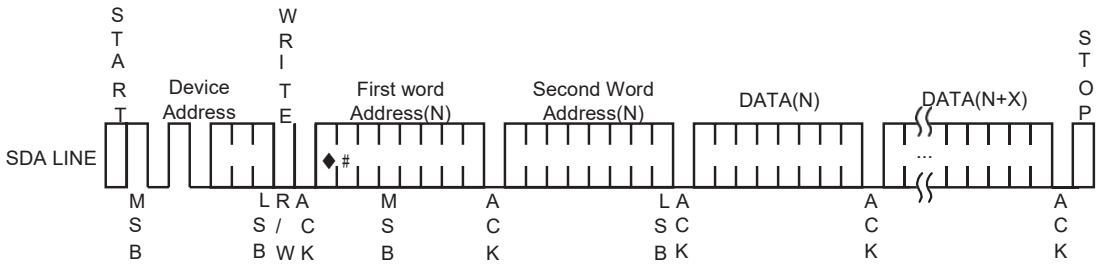
(B) PAGE WRITE

The 128K/256K EEPROM are capable of 64-byte page write.

A page write is initiated the same way as a byte write, but the microcontroller does not send a STOP condition after the first data word is clocked in. The microcontroller can transmit up to 63 more data words after the EEPROM acknowledges receipt of the first data word. The EEPROM will respond with a "0" after each data word is received. The microcontroller must terminate the page write sequence with a STOP condition (see Figure 4).

The lower five bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. If more than 64 data words are transmitted to the EEPROM, the data word address will "roll over" and the previous data will be overwritten.

Figure 4: Page Write



Notes:

1) *=Don't care bits
2) #=Don't care bits for HK24C128

(C) ACKNOWLEDGE POLLING

ACKNOWLEDGE polling may be used to poll the programming status during a self-timed internal programming. By issuing a valid read or write address command, the EEPROM will not acknowledge at the 9th clock cycle if the device is still in the self-timed programming mode. However, if the programming completes and the chip has returned to the STANDBY mode, the device will return a valid ACKNOWLEDGE

signal at the 9th clock cycle.

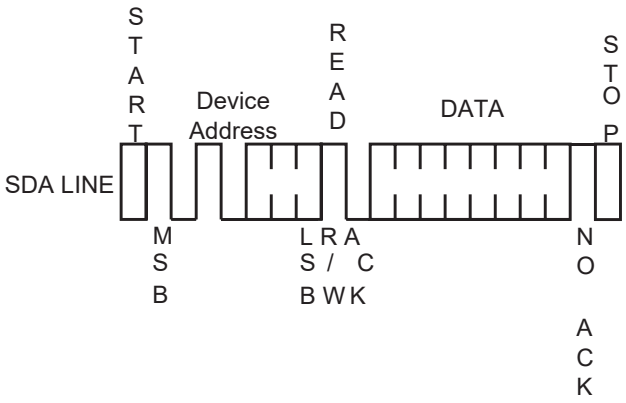
7. READ OPERATIONS

The read command is similar to the write command except the 8th read/write bit in address word is set to “1”. The three read operation modes are described as follows:

(A) CURRENT ADDRESS READ

The EEPROM internal address word counter maintains the last read or write address plus one if the power supply to the device has not been cut off. To initiate a current address read operation, the microcontroller issues a START bit and a valid device address word with the read/write bit (8th) set to “1”. The EEPROM will response with an ACKNOWLEDGE signal on the 9th serial clock cycle. An 8-bit data word will then be serially clocked out. The internal address word counter will then automatically increase by one. For current address read the micro-controller will not issue an ACKNOWLEDGE signal on the 18th clock cycle. The micro-controller issues a valid STOP bit after the 18th clock cycle to terminate the read operation. The device then returns to STANDBY mode(Figure 5).

Figure 5: Current Address Read



Notes:

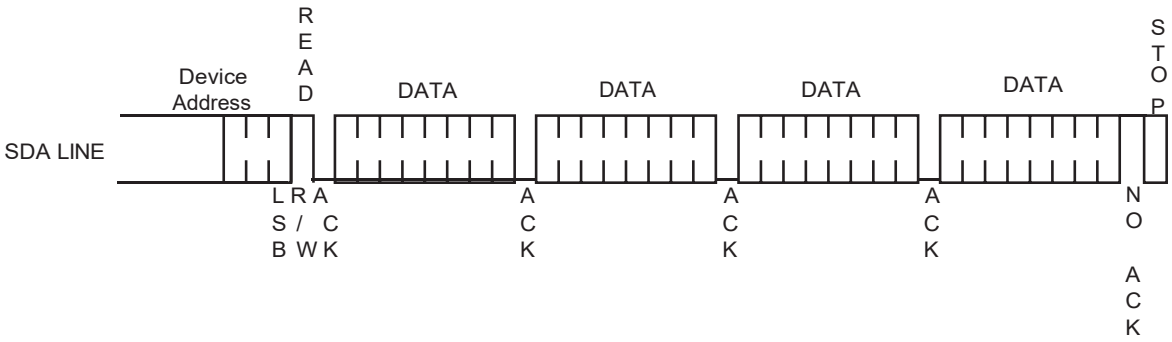
1) *=Don’t care bits
2) #=Don’t care bits for HK24C128

(B) SEQUENTIAL READ

The sequential read is very similar to current address read. The micro-controller issues a START bit and a valid device address word with read/write bit (8th) set to “1”. The EEPROM will response with an ACKNOWLEDGE signal on the 9th serial clock cycle. An 8-bit data word will then be serially clocked out. Meanwhile the internally address word counter will then automatically increase by one. Unlike current address read, the micro-controller sends an ACKNOWLEDGE signal on the 18th clock cycle signaling the EEPROM device that it wants another byte of data. Upon receiving the ACKNOWLEDGE signal, the EEPROM will serially clocked out an 8-bit data word based on the incremented internal address counter. If the micro-controller needs

another data, it sends out an ACKNOWLEDGE signal on the 27th clock cycle. Another 8-bit data word will then be serially clocked out. This sequential read continues as long as the micro-controller sends an ACKNOWLEDGE signal after receiving a new data word. When the internal address counter reaches its maximum valid address, it rolls over to the beginning of the memory array address. Similar to current address read, the micro-controller can terminate the sequential read by not acknowledging the last data word received, but sending a STOP bit afterwards instead (Figure 6).

Figure 6: Sequential Read



Notes:

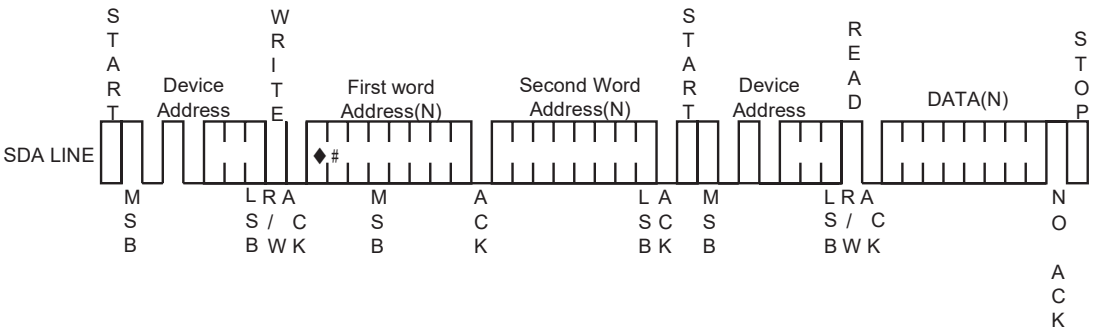
1) *=Don’t care bits
2) #=Don’t care bits for HK24C128

(C) RANDOM READ

Random read is a two-steps process. The first step is to initialize the internal address counter with a target read address using a “dummy write” instruction. The second step is a current address read.

To initialize the internal address counter with a target read address, the micro-controller issues a START bit first, follows by a valid device address with the read/write bit (8th) set to “0”. The EEPROM will then acknowledge. The micro-controller will then send the address word. Again the EEPROM will acknowledge. Instead of sending a valid written data to the EEPROM, the micro-controller performs a current address read instruction to read the data. Note that once a START bit is issued, the EEPROM will reset the internal programming process and continue to execute the new instruction - which is to read the current address (Figure 7).

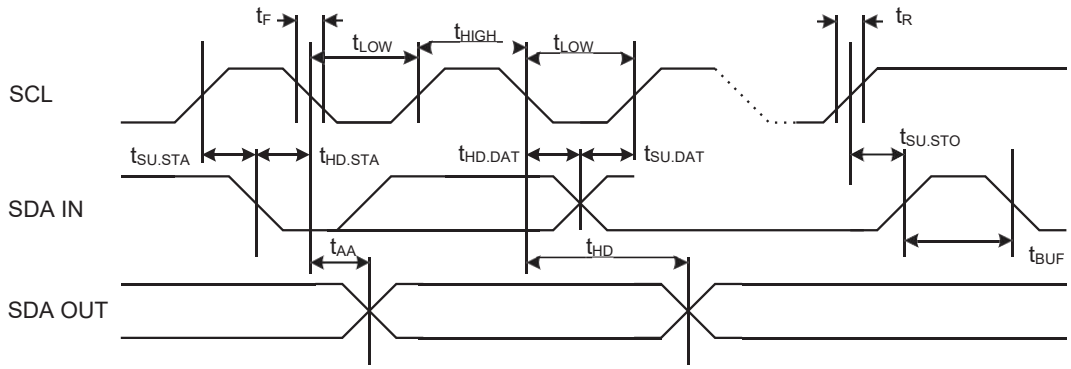
Figure 7: Random Read



Notes:

1) *=Don’t care bits
2) #=Don’t care bits for HK24C128

Figure 8: SCL and SDA Bus Timing



8. Table-A AC CHARACTERISTICS

Symbol	Parameter	1.8V		2.5V		Unit
		Min	Max	Min	Max	
f_{SCL}	Clock frequency, SCL		400		1000	kHz
t_{LOW}	Clock pulse width low	1.2		0.7		μs
t_{HIGH}	Clock pulse width high	0.4		0.3		μs
t_I	Noise suppression time(1)		100		50	ns
t_{AA}	Clock low to data out valid	0.3	0.9	0.2	0.7	μs
t_{BUF}	Time the bus must be free before a new transmission can start(1)	1.3		0.5		μs
$t_{HD.STA}$	START hold time	0.6		0.25		μs
$t_{SU.STA}$	START set-up time	0.6		0.25		μs
$t_{HD.DAT}$	Data in hold time	0		0		μs
$t_{SU.DAT}$	Data in set-up time	100		100		ns
t_R	Input rise time(1)		0.3		0.3	μs
t_F	Input fall time(1)		300		100	ns
$t_{SU.STO}$	STOP set-up time	0.6		0.25		μs
t_{DH}	Date out hold time	100		50		ns
t_{WR}	Write cycle time		5		5	ms
Endurance(1)	25℃, Page Mode, 3.3V	1,000,000				Write Cycles

Notes:

1. This Parameter is expected by characterization but are not fully screened by test.
2. AC Measurement conditions:

   R_L (Connects to Vcc): 1.3KΩ

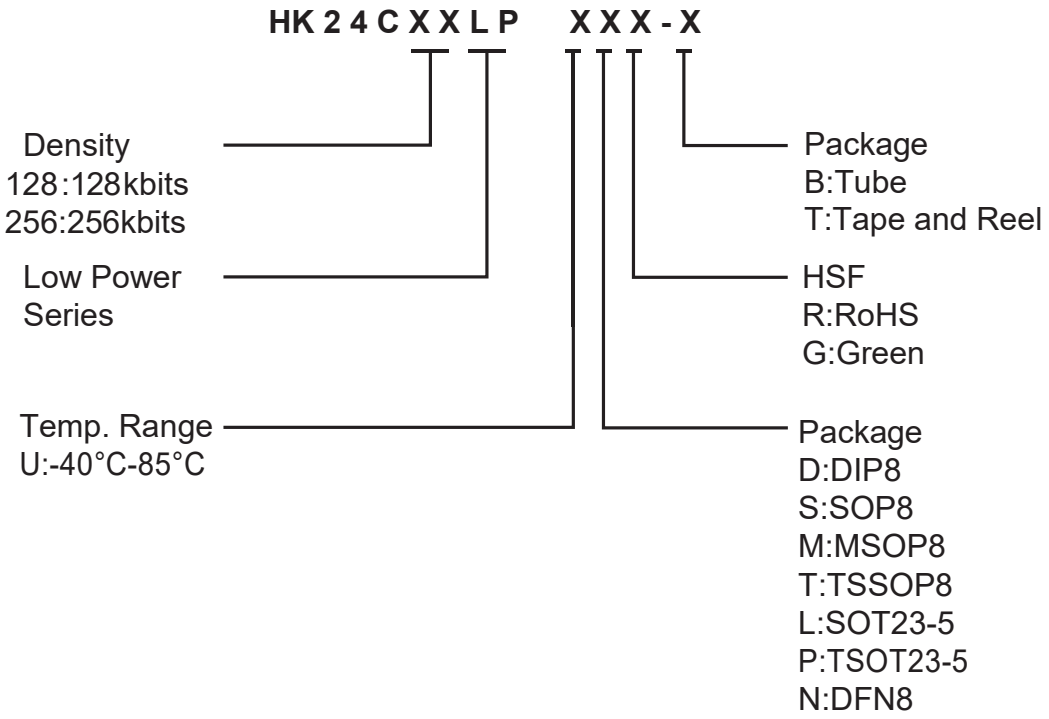
   Input Pulse Voltages: 0.3Vcc to 0.7Vcc

   Input and output timing reference Voltages: 0.5Vcc

9. Table-B DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typical	Max	Unit
VCC1	Power supply		1.8		5.5	V
ICC	Supply read current	VCC @ 5.0V SCL = 400 kHz		0.5	1	mA
ICC	Supply write current	VCC @ 5.0V SCL = 400 kHz		0.5	1	mA
ISB1	Supply current	VCC @ 1.8V, VIN = VCC or VSS			1	μA
ISB2	Supply current	VCC @ 2.5V, VIN = VCC or VSS			1	μA
ISB3	Supply current	VCC @ 5.0V, VIN = VCC or VSS		0.03	1	μA
IIL	Input leakage current	VIN = VCC or VSS			3	μA
ILO	Output leakage current	VIN = VCC or VSS			3	μA
VIL	Input low level		-0.6		VCCx0.3	V
VIH	Input high level		VCCx0.7		VCC+0.5	V
VOL1	Output low level	VCC @ 1.8V, IOL = 0.15 mA			0.2	V
VOL2	Output low level	VCC @ 3.0V, IOL = 2.1 mA			0.4	V

10. ORDERING INFORMATION:

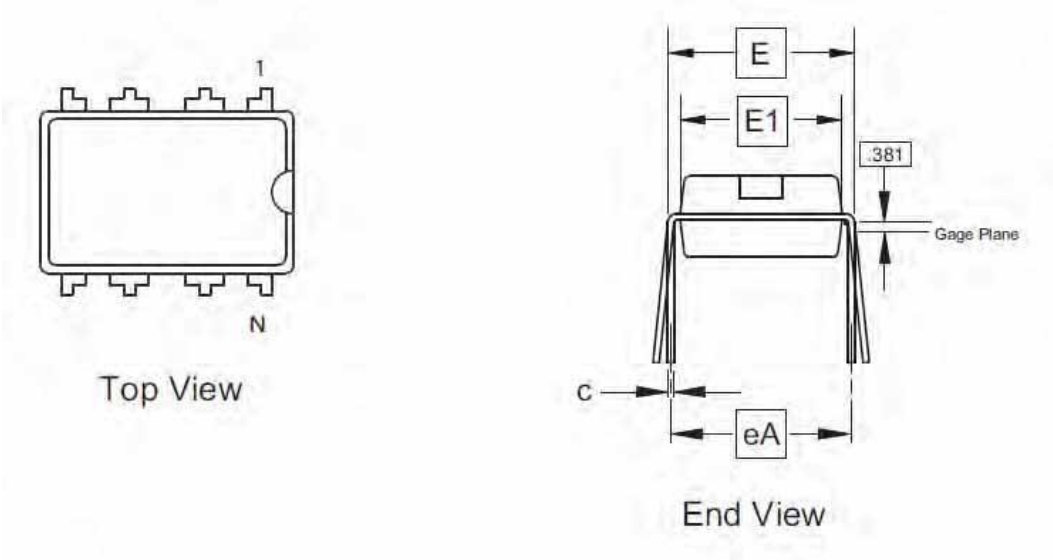


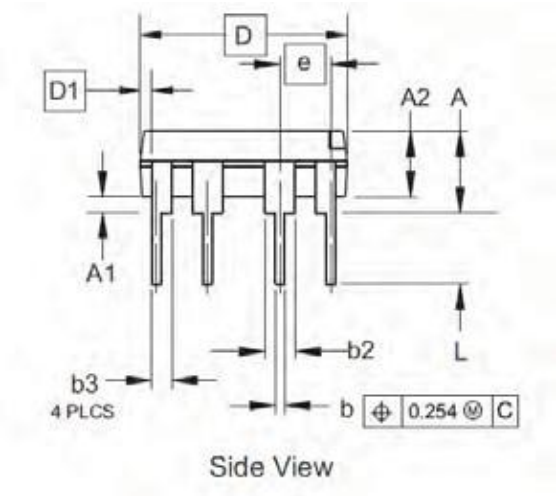
Density	Package	Temperature Range	VCC	HSF	Packaging	Ordering Code
128Kbits	DIP8	-40℃-85℃	1.8V-5.5V	RoHS	Tube	HK24C128-UDR-B
				Green	Tube	HK24C128-UDG-B
	SOP8	-40℃-85℃	1.8V-5.5V	RoHS	Tube	HK24C128-USR-B
					Tape and Reel	HK24C128-USR-T
				Green	Tube	HK24C128-USG-B
					Tape and Reel	HK24C128-USG-T
	MSOP8	-40℃-85℃	1.8V-5.5V	RoHS	Tube	HK24C128-UMR-B
					Tape and Reel	HK24C128-UMR-T
				Green	Tube	HK24C128-UMG-B
					Tape and Reel	HK24C128-UMG-T
	TSSOP8	-40℃-85℃	1.8V-5.5V	RoHS	Tube	HK24C128-UTR-B
					Tape and Reel	HK24C128-UTR-T
				Green	Tube	HK24C128-UTG-B
					Tape and Reel	HK24C128-UTG-T
	SOT23-5	-40℃-85℃	1.8V-5.5V	RoHS	Tape and Reel	HK24C128-ULR-T
				Green	Tape and Reel	HK24C128-ULG-T
	TSOT23-5	-40℃-85℃	1.8V-5.5V	RoHS	Tape and Reel	HK24C128-UPR-T
				Green	Tape and Reel	HK24C128-UPG-T
	DFN8	-40℃-85℃	1.8V-5.5V	RoHS	Tape and Reel	HK24C128-UNR-T
				Green	Tape and Reel	HK24C128-UNG-T

Density	Package	Temperature Range	VCC	HSF	Packaging	Ordering Code
256Kbits	DIP8	-40℃-85℃	1.8V-5.5V	RoHS	Tube	HK24C256-UDR-B
				Green	Tube	HK24C256-UDG-B
	SOP8	-40℃-85℃	1.8V-5.5V	RoHS	Tube	HK24C256-USR-B
					Tape and Reel	HK24C256-USR-T
				Green	Tube	HK24C256-USG-B
					Tape and Reel	HK24C256-USG-T
	MSOP8	-40℃-85℃	1.8V-5.5V	RoHS	Tube	HK24C256-UMR-B
					Tape and Reel	HK24C256-UMR-T
				Green	Tube	HK24C256-UMG-B
					Tape and Reel	HK24C256-UMG-T
	TSSOP8	-40℃-85℃	1.8V-5.5V	RoHS	Tube	HK24C256-UTR-B
					Tape and Reel	HK24C256-UTR-T
				Green	Tube	HK24C256-UTG-B
					Tape and Reel	HK24C256-UTG-T
	SOT23-5	-40℃-85℃	1.8V-5.5V	RoHS	Tape and Reel	HK24C256-ULR-T
				Green	Tape and Reel	HK24C256-ULG-T
	TSOT23-5	-40℃-85℃	1.8V-5.5V	RoHS	Tape and Reel	HK24C256-UPR-T
				Green	Tape and Reel	HK24C256-UPG-T
	DFN8	-40℃-85℃	1.8V-5.5V	RoHS	Tape and Reel	HK24C256-UNR-T
				Green	Tape and Reel	HK24C256-UNG-T

11. Packaging Information

11.1 DIP8 PACKAGE OUTLINEDIMENSIONS





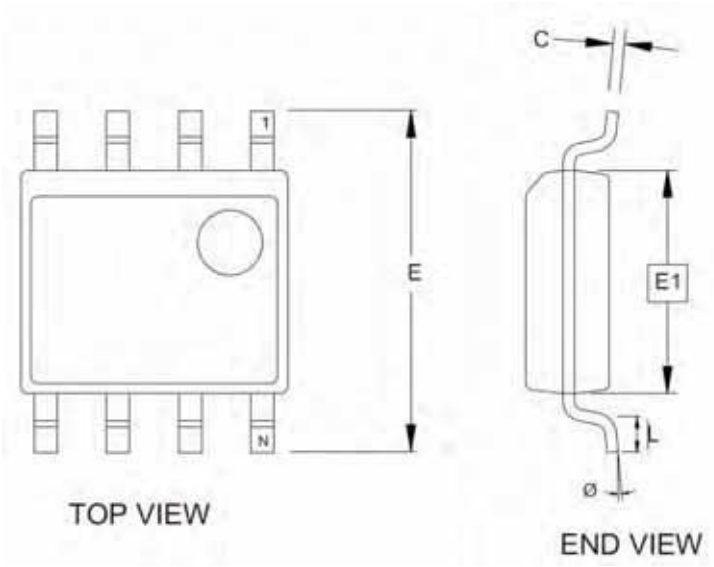
Notes:

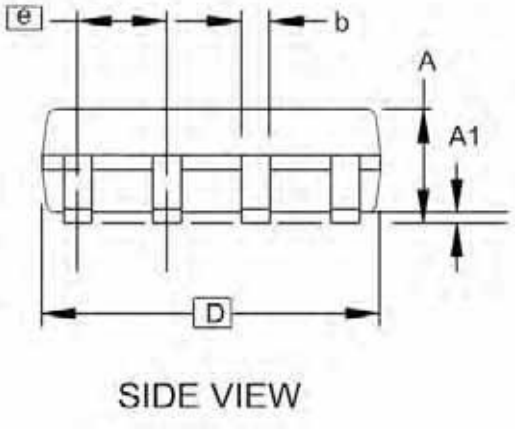
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
4. E and eA measured with the leads constrained to be perpendicular to datum.
5. Pointed or rounded lead tips are preferred to ease insertion.
6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	5.334	2
A1	0.381	-	-	
A2	2.921	3.302	4.953	
b	0.356	0.457	0.559	5
b2	1.143	1.524	1.778	6
b3	0.762	0.991	1.143	6
c	0.203	0.254	0.356	
D	9.017	9.271	10.16	3
D1	0.127	0	0	3
E	7.62	7.874	8.255	4
E1	6.096	6.35	7.112	3
e	2.54 BSC			
eA	7.62 BSC			4
L	2.921	3.302	3.81	2

11.2 SOP8 PACKAGE OUTLINEDIMENSIONS





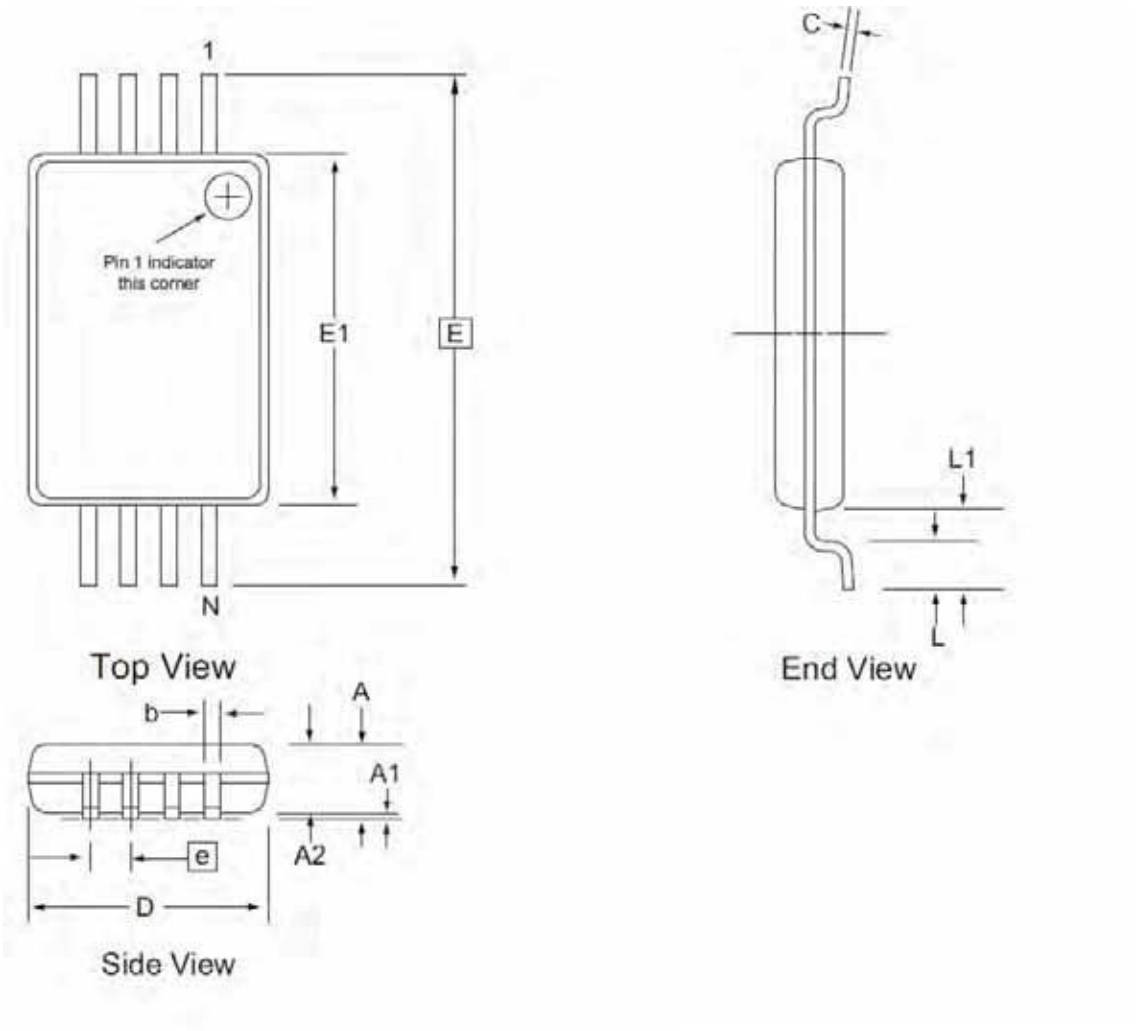
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX
A1	0.10	–	0.25
A	1.35	–	1.75
b	0.31	–	0.51
C	0.17	–	0.25
D	4.80	–	5.05
E1	3.81	–	3.99
E	5.79	–	6.20
e	1.27 BSC		
L	0.40	–	1.27
Ø	0°	–	8°

Notes:

This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

11.3 TSSOP8 PACKAGE OUTLINEDIMENSIONS



Notes:

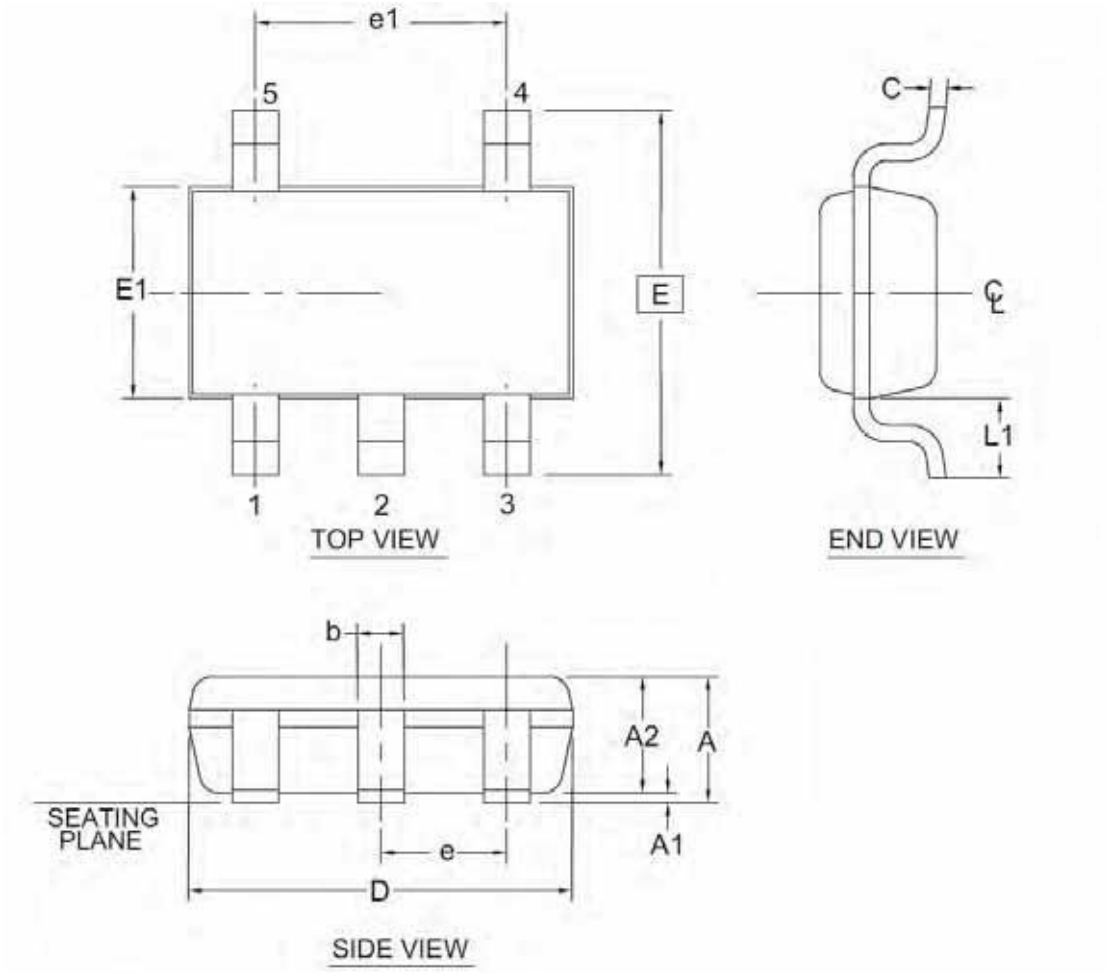
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm(0.010in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension D and E1 to be determined at Datum Plane H.

COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.2	
A1	0.05	-	0.15	
A2	0.8	1	1.05	
D	2.9	3	3.1	2,5
E	6.4 BSC			
E1	4.3	4.4	4.5	3,5
b	0.19	0.25	0.3	4
e	0.65 BSC			
L	0.45	0.6	0.75	
L1	1.00 REF			
C	0.09	-	0.2	

11.4 SOT-23-5 PACKAGE OUTLINE DIMENSIONS



Notes:

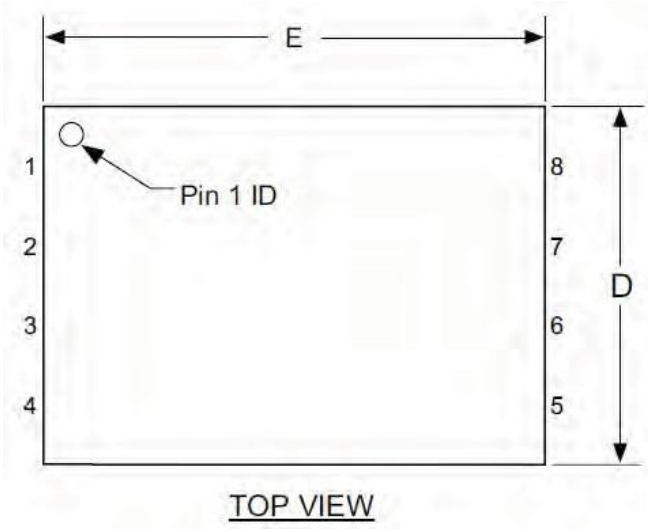
1. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.15 mm per side.
2. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
3. These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.
4. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 mm total in excess of the "b" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and an adjacent lead shall not be less than 0.07 mm.

This drawing is for general information only. Refer to JEDEC Drawing MO-193, Variation AB for additional information.

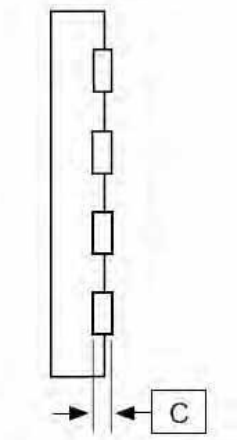
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1	
A1	0	-	0.1	
A2	0.7	0.9	1	
c	0.08	-	0.2	3
D	2.9 BSC			1,2
E	2.8 BSC			1,2
E1	1.6 BSC			1,2
L1	0.6 BSC			
e	0.95 BSC			
e1	1.9 BSC			
b	0.3	-	0.5	3,4

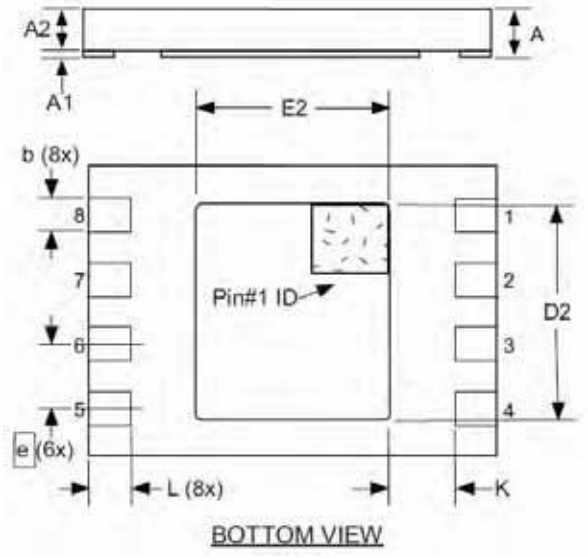
11.5 DFN8 PACKAGE OUTLINE DIMENSIONS



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Notes:

1. This drawing is for general information only. Refer toDrawing MO-229, for proper dimensions, tolerances, datums, etc.
2. The Pin #1 ID is a laser-marked feature on Top View.
3. Dimensions b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.
4. The Pin #1 ID on the Bottom View is an orientationfeature on the thermal pad..

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.50	0.55	0.60	
A1	0.00	0.02	0.05	
A2	-	-	0.55	
D	1.90	2.00	2.10	
D2	1.40	1.50	1.60	
E	2.90	3.00	3.10	
E2	1.20	1.30	1.40	
b	0.18	0.25	0.30	3
C	1.52 REF			
L	0.30	0.35	0.40	
e	0.5 BSC			
K	0.20	-	-	